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Paper 9
Entered: August 11, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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GSI TECHNOLOGY, INC.,
Petitioner,

v.

CYPRESS SEMICONDUCTOR CORPORATION,
Patent Owner.

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IPR2014-00419
Patent 6,967,861 B2

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Before WILLIAM V. SAINDON, MIRIAM L. QUINN, and KEVIN W. CHERRY, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
*37 C.F.R. § 42.108*

# I. INTRODUCTION

## *A. Background*

Petitioner filed a corrected Petition requesting an *inter partes* review of claims 1–3, 9–11, 17–20, 26–28, and 34 of U.S. Patent No. 6,967,861 B2 (Ex. 1001, "the '861 patent"). Paper 4 ("Pet."). Patent Owner timely filed a Preliminary Response. Paper 8 ("Prelim. Resp."). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

> THRESHOLD.—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Petitioner contends that the challenged claims are unpatentable under 35 U.S.C. §§ 102 and 103 based on the following specific grounds:

| **Reference(s)** | **Basis** | **Claims Challenged** |
|---|---|---|
| Takahashi[1] | § 102 | 1, 9, 18, 26 |
| Takahashi | § 103 | 2, 3, 10, 11, 19, 20, 27, 28 |
| Takahashi and Tsuchida[2] | § 103 | 17, 34 |
| Okuyama[3] and either Takahashi or Tsuchida | § 103 | 1–3, 9–11, 17–20, 26–28, 34 |

For the reasons given below, we do not institute an *inter partes* review of any challenged claim.

[1] U.S. Patent No. 7,162,657 B2 (issued Jan. 9, 2007) (Ex. 1003).
[2] U.S. Patent No. 6,647,478 B2 (issued Nov. 11, 2003) (Ex. 1005).
[3] JP App. 2000-173270 (published June 23, 2000) (Ex. 1004). An English-language translation was filed as Exhibit 1007 (hereinafter "Ex. 1007" or "Okuyama"). We will cite to the translation.

### *B. Related Matters*

In addition to this proceeding, Petitioner has filed petitions challenging the patentability of certain claims of Patent Owner's U.S. Patent No. 6,292,403 (IPR2014-00121); U.S. Patent No. 6,069,839 (IPR2014-00202); U.S. Patent No. 6,445,645 (IPR2014-00426); and U.S. Patent No. 6,385,128 (IPR2014-00427). In addition, Petitioner states that it is subject to a patent infringement suit brought by Patent Owner in *Cypress Semiconductor Corp. v. GSI Technology, Inc.*, Case Nos. 3:13-cv-02013-JST, 4:13-cv-03757-JST (N.D. Cal.). Pet. 2.

### *C. The Challenged Patent*

The '861 patent involves memory devices such as Quad Data Rate ("QDR") Static Random Access Memory ("SRAM") devices. Ex. 1001, 1:7–10. In a typical QDR SRAM device, data is read on a first half of a clock cycle and data is written on the second half of the clock cycle. *Id.* at 1:49–53. According to the '861 patent, each read/write operation in the prior art is performed completely within its respective half of the clock cycle. *Id.* at 1:53–58. Thus, upon commencing the write portion of the clock cycle, a prior art SRAM device receives an address to which data may be written and then writes data to that write address. *See id.*, Fig. 1 (depicting a prior art read/write cycle). The result of this is a longer cycle due to the delay between the read operation and the write operation, caused by having to receive a write address to which to write. *See id.*

The '861 patent, in contrast, allows the write operation to commence immediately after the read operation by using a write address captured during a prior clock cycle, rather than during the same clock cycle as in the prior art. *Id.* at 2:6–11; *see also id.* at 3:24–29 ("Briefly stated, an improvement in the cycle time is achieved by . . . write addresses and data . . . captured and buffered during a

given read to write cycle are actually written in the next read to write cycle"). By using a write address captured during a prior clock cycle, the device does not have to wait for the write address to be received and decoded within the same clock cycle. *See id.* at 2:55–65. Instead, because the device uses a write address gathered during a prior clock cycle, that write address will be decoded by the time the read portion of the current clock cycle has finished. *See id.* Put another way, the write address received in a given clock cycle is not written to in that clock cycle, but rather in a subsequent clock cycle.

Of the claims challenged, claims 1, 9, 18, and 26 are independent. Claim 1 is illustrative of the claimed subject matter, and is reproduced below:

> 1. A method for implementing a self-timed, read to write operation in a memory storage device, the method comprising:
> capturing a read address during a first half of a current clock cycle;
> commencing a read operation so as to read data corresponding to said captured read address onto a pair of bit lines;
> ***commencing a write operation*** for said current clock cycle so as to cause write data to appear on said pair of bit lines as soon as said read data from said captured read address is amplified by a sense amplifier, ***wherein said write operation uses a previous write address captured during a preceding clock cycle***; and
> ***capturing a current write address*** during a second half of said current clock cycle, said current write address ***to be used for a write operation implemented during a subsequent clock cycle***;
> wherein said commencing a write operation for said current clock cycle is timed independent of said current write address captured during said second half of said current clock cycle.

*Id*. at 5:34–55 (emphases added to highlight limitations at issue).

### *D. Claim Construction*

We interpret claims of an unexpired patent using the broadest reasonable interpretation in light of the specification of the patent. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner proposes an interpretation of the phrase "as soon as," found in each challenged claim. Pet. 9. Patent Owner proposes a different interpretation and argues that the interpretation of the phrase is unnecessary for purposes of this decision. Prelim. Resp. 8–11. We agree with Patent Owner that express construction of this phrase is unnecessary for purposes of this Decision, because no issue in this Decision turns on this phrase.

Patent Owner proposes an interpretation for the "wherein" clause found at the end of each of the independent claims. Prelim. Resp. 12–14. Express construction of this phrase is unnecessary for purposes of this Decision, because no issue in this Decision turns on the proper construction for this clause.

## II. ANALYSIS

### *A. Overview*

Each of the challenged claims requires that the write address received in a given clock cycle is not the write address used in that clock cycle and, complimentary to this, that the write address used in that clock cycle was received in a prior clock cycle. Each of Petitioner's grounds of unpatentability rely on Takahashi to describe these features, but, as is explained in greater detail below,

Petitioner has not shown sufficiently that Takahashi describes these features. In effect, while Takahashi discloses a write operation immediately following a read operation, Takahashi enables this not by using a previously gathered write address, but by overlapping the read and write cycles and writing at the same time as selecting the word line.

### *B. Takahashi Anticipation Ground: Claims 1, 9, 18, and 26*

#### *1. Overview of Takahashi (Ex. 1003)*

Takahashi describes a method for controlling semiconductor storage devices, such as a QDR SRAM. Ex. 1003, 1:6–9, 13–32. The reading and writing of the memory device alternate; in some embodiments reading and writing is performed in one clock cycle (*see, e.g., id.* at Figs. 3B, 6, 7B, 12) and in other embodiments, reading and writing are performed in alternating clock cycles (*see, e.g., id.* at Figs. 15, 16B). Takahashi describes the read and write cycles involve the following steps:

> The ***read cycle*** is comprised of the decoding of the read address, selection of the word line and the cell, and activation of the sense amplifier, while the ***write cycle*** is comprised of the decoding of the write address, selection of the word line, activation of the write amplifier and pre-charging of the bit line.

*Id.* at 11:26–31 (emphases added). An address identifies a particular cell in the memory array, using X and Y coordinates. *Id.* at 2:2–3. Decoding is the process of converting the address into the particular X and Y coordinates of a cell. *See id.* at 12:39–43. A particular cell is selected by enabling gates at its X coordinate (i.e., its word line) and Y coordinate. *Id.* at 18:30–31. This exposes the cell, via a bit line, to either the sense amplifier (if the cell is being read) or the write amplifier (if

the cell is being written). *Id.* at 18:30–36 (describing a read operation); 19:44–59 (describing a write operation).

Takahashi describes that the read and write cycles are overlapped, which shortens the overall read/write cycle. *Id.* at 12:9–11. The overlap of the read and write cycles occurs by performing the activation of the sense amplifier while the write address is being decoded, such that as soon as the read operation finishes (i.e., when the bit line is free), the write address will be decoded. Figure 1 of Takahashi depicts this overlap and is reproduced below:

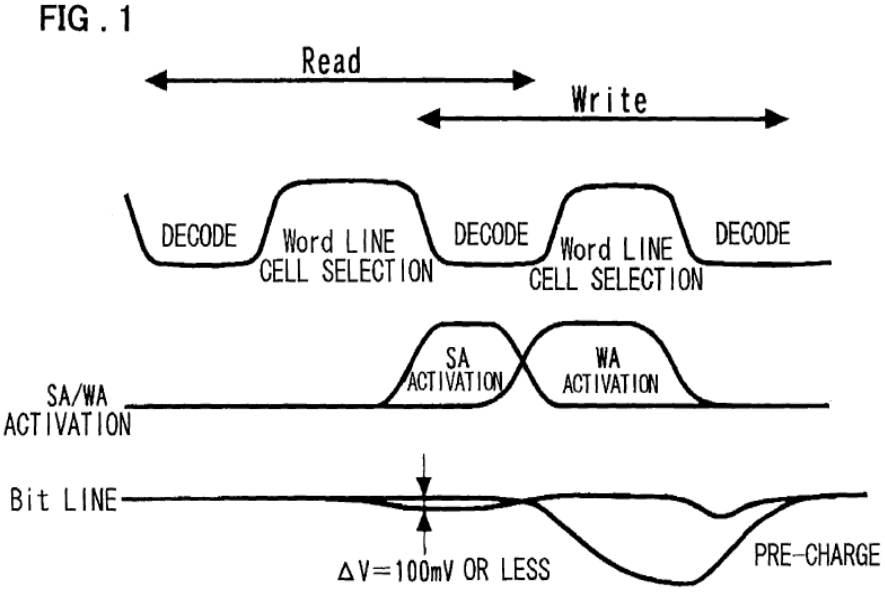


Figure 1 of Takahashi depicts a read/write cycle where the decoding of the write address occurs while the sense amplifier reads from the read address. *Id.* at 11:35–38. From left to right, i.e., as time moves forward, Figure 1 shows a read address is decoded and then a word line is enabled to select a cell for reading. After that, a write address is decoded and then a word line is enabled to select a cell for writing. This cycle continues with the next read address decoded, a cell selected, and so on. Figure 1 also shows that, while the write address is being decoded, a sense

amplifier (SA) is reading the bit line (i.e., reading from the cell previously selected). After the sense amplifier becomes deactivated, the write amplifier (WA) is activated and a write operation begins on the bit line to the selected word line. Figure 1 further shows that, after writing to the cell, the write amplifier is turned off and the bit line is reset ("pre-charge[d]") to allow the next read operation to commence.

In addition to shortening the read/write cycle by overlapping read and write cycles, Takahashi shortens the write cycle by activating the write amplifier before the particular cell to be written to (specified by the write address) is fully selected, in effect writing to the cell while it is being selected. *Id.* at 19:10–44; *see also* Fig. 11 (depicting how the Takahashi device is able to write to a cell at the same time it is being selected). This is depicted in Figure 1 by the activation of the write amplifier, word line/cell, and bit line all at nearly the same time.

*2. Overview of Petitioner's Ground*

Independent claim 1 requires a read-to-write operation in a memory including a step of "commencing a write operation . . . wherein said write operation uses a previous write address captured during a preceding clock cycle" and then, relatedly, "capturing a current write address during . . . said current clock cycle . . . to be used for a write operation implemented during a subsequent clock cycle." Thus, in a given clock cycle, the claim recites two separate write addresses: the first is the write address *used* to write in a cell during the current clock cycle and the second is the write address *received* during the current clock cycle. The first write address was received in a prior clock cycle, and is used in the current cycle. The second write address is received in the current cycle, and is used in a later clock cycle.

Petitioner labels these limitations as "[1 d]" and "[1 e]," respectively, which we likewise use, for consistency. We address Petitioner's assertions with respect to each, in turn.

*3. Limitation [1 d]: Writing Using a Prior Write Address*

With respect to limitation [1 d], requiring commencing a write operation using a write address gathered during a prior clock cycle, Petitioner alleges that Figure 15 of Takahashi discloses "the write operation for the current clock cycle uses a previous write address captured during a preceding clock cycle, while the write address A2 . . . is used in the next clock cycle." Pet. 17–18. Figure 15 of Takahashi is reproduced below.

FIG .15

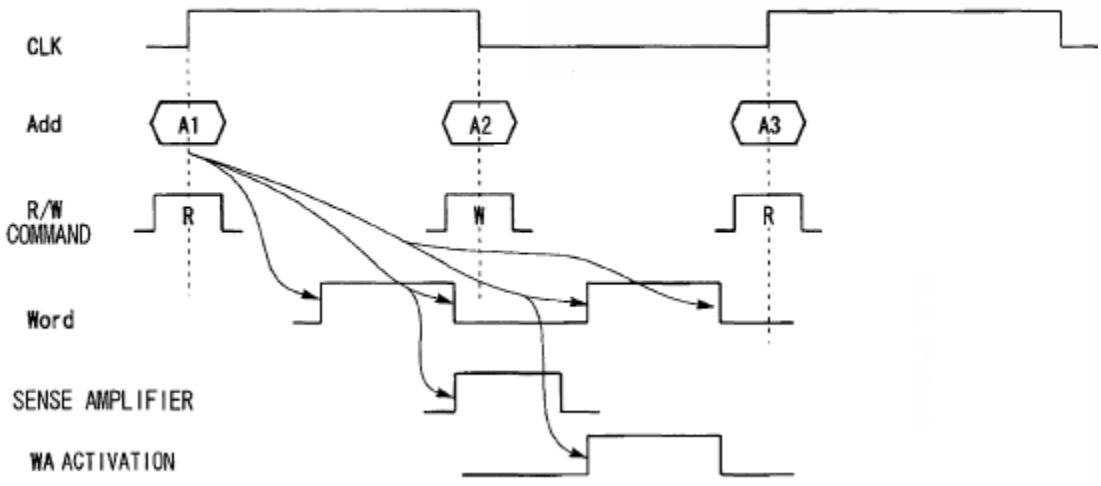


Figure 15 of Takahashi depicts a timing diagram for an alternative embodiment of Takahashi. Ex. 1003, 7:1–2. Takahashi explains that "the read command RE and addresses A1 and A3 are sampled with the rising edge of the clock signal CLK, while the write command W and the address A2 are sampled with the falling edge." *Id.* at 21:10–13.

Petitioner does not explain the factual or technical basis for its assertion that the write operation shown in Figure 15 uses an address gathered in a previous clock cycle (i.e., was gathered in a clock cycle prior to that shown in Figure 15). Petitioner cites to no portion of Takahashi that states as much, nor does Petitioner explain the citations it does provide. *See* Pet. 17–18 (discussing limitation [1 d]) (citing Ex. 1003, 4:44–49, 9:28–37, 21:6–17, Fig. 15).

Reviewing Petitioner's cited passages, we do not find a discussion of using a write address from a previous clock cycle. The passage Petitioner cited at column 4 discuss the sequence of the write cycle, but does not mention the write address being gathered in a previous cycle. *See also* Prelim. Resp. 18 (arguing that Petitioner's citation to column 4 is unavailing). The passage Petitioner cited at column 9 merely discusses how the read and write operations alternate. *See also id.* at 18–19 (arguing that Petitioner's citation to column 9 is unavailing). The passage Petitioner cited at column 21 discusses that both edges of a clock cycle are used to trigger read/write commands (i.e., that read and write both occur in one clock cycle). *See also id.* at 17–18 (arguing that Petitioner's citation to column 21 is unavailing). Reviewing these passages, we are persuaded that Petitioner has not supported sufficiently its assertion that Takahashi discloses using a write address from a previous clock cycle.

Moreover, Petitioner fails to explain the disclosure in Takahasi contrary to the contention that it discloses using a write address from a previous cycle. Specifically, Figure 15 of Takahashi shows a progression of receiving a write address, decoding a write address, and then performing a write operation to a write address. *Compare* Ex. 1003, Figs. 1 & 11 (showing Takahashi's process of decoding a write address and then performing a write operation by selecting a word line at nearly the same time as activating the write amplifier) *with id.*, Fig. 15

(depicting the same pattern). Absent sufficient evidence or technical analysis from Petitioner to the contrary, Takahashi, therefore, does not appear to disclose that the write address used in the clock cycle was gathered in a prior clock cycle, as required by claim 1, but rather that a single write address is both received and then used in one clock cycle.

Accordingly, given the lack of sufficiency of Petitioner's showing on this record, we are not persuaded by Petitioner's assertion that Takahashi discloses limitation [1 d], which requires commencing a write operation using a write address gathered during a prior clock cycle.

*4. Limitation [1 e]: Capturing a Write Address for a Later Clock Cycle*

With respect to limitation [1 e], requiring a step of capturing a write address to be used in a later clock cycle, Petitioner relies on Figure 7A of Takahashi. Pet. 20–21. Figures 7A and 7B are reproduced below:

FIG . 7A

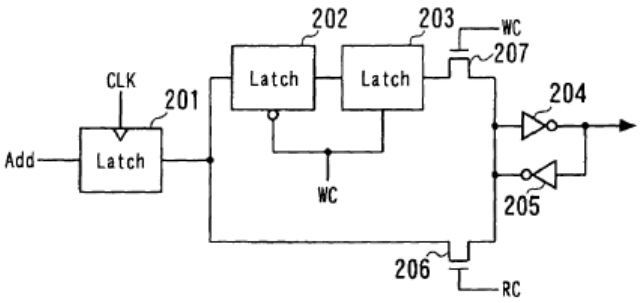


FIG . 7B

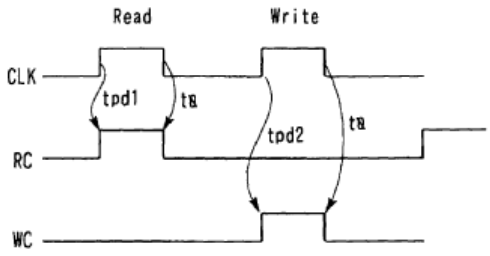


Figure 7A of Takahashi depicts a circuit for introducing delays in an address register. Ex. 1003, 6:46–48, 17:9–14. Figure 7B depicts a timing diagram for illustrating the timing of the circuit in Figure 7A. *Id.* at 6:47–48.

Petitioner asserts that, because of latches 202 and 203, "the write address path has a one-clock-cycle delay relative to the read address path." Pet. 20–21.

Thus, Petitioner asserts, "the captured write address will be used for a write operation implemented during a subsequent clock cycle." Pet. 21 (citing Ex. 1003, 17:9–34). Claim 1 requires performing a read and a write operation in the same clock cycle, however, whereas the address register in Figure 7A only performs one operation per clock cycle, as shown in Figure 7B. Ex. 1003, 17:12–14 ("FIG. 7B shows the timing of the clock[s] . . . in FIG. 7A"). Thus, the address register circuit in Figure 7A is not configured in the manner required by claim 1. *See Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (anticipation requires a prior art reference "must not only disclose all elements of the claim within the four corners of the document, *but must also disclose those elements arranged as in the claim*.") (internal quotations omitted, emphasis added).

Petitioner also points back to Figure 15, in which a single clock cycle includes read and write operations. Pet. 21. Figures 7 and 15, however, are directed to different embodiments, one performing a read/write cycle on separate clock cycles, and one performing a read/write cycle in a single clock cycle. An anticipation analysis cannot seek to combine separate and distinct embodiments. *See Net MoneyIN*, 545 F.3d at 1371 ("it is not enough that the prior art reference … includes multiple, distinct teachings that [an ordinary] artisan might somehow combine to achieve the claimed invention."); *see also* Ex. 1003 at 21:3–5 ("FIG. 15 depicts . . . *a further modification* of the present invention.") (emphasis added). Accordingly, we determine that Petitioner has not shown sufficiently on this record that Takahashi anticipates the subject matter of claim 1.

Petitioner relies on these insufficient findings with respect to similar limitations in independent claims 9, 18, and 26. In view of the discussion above, Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that Takahashi anticipates the subject matter of claims 1, 9, 18, and 26.

*C. Takahashi Obviousness Ground: Claims 2, 3, 10, 11, 19, 20, 27, and 28; Takahashi and Tsuchida Obviousness Ground: Claims 17 and 34*

The claims challenged in these grounds depend from claim 1, 9, 18, or 26. Petitioner relies on the insufficient evidence discussed above with respect to claims 1, 9, 18, and 26 in the Takahashi obviousness ground and the Takahashi and Tsuchida obviousness ground. Pet. 26 ("Takahashi discloses each element of claims 1, 9, 18, and 26 as set forth . . . above"); *id.* at 33 ("Takahashi . . . discloses all of the elements of claims 9 and 26"); *id.* at 41 ("Takahashi . . . discloses a write operation that uses a previous write address . . . . *See* Challenge #1, claim [1 d]"). Accordingly, these grounds have the same evidentiary deficiencies identified in our discussion of claims 1, 9, 18, and 26 above.

Thus, Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that the subject matter of claims 2, 3, 10, 11, 19, 20, 27, and 28 is unpatentable over Takahashi or that the subject matter of claims 17 and 34 is unpatentable over Takahashi and Tsuchida

*D. Okuyama, Alone or In Combination with Takahashi or Tsuchida: All Challenged Claims*

With respect to the Okuyama obviousness ground, Petitioner offers two theories with respect to limitations [1 d] and [1 e]. First, Petitioner purports to address these limitations by asserting that it would have been "obvious to implement the memory in Okuyama as a late write part." Pet. 40–41 (citing Ex. 1006 ¶ 25, which repeats the language in the petition); *id.* at 43. Petitioner asserts that a "late write" "embodies [the] principle [claimed]" and that changing from the conventional-write-type memory of Okuyama to a late-write-type memory would have been "predictable to a person of ordinary skill." *Id.* at 40–41. Petitioner, however, provides only the barest of explanations of what "late write" means and

as well as only conclusory evidence and analysis as to how a "late write" would satisfy limitations [1 d] and [1 e]. *See id.* Thus, Petitioner's bare assertion is insufficient to demonstrate a reasonable likelihood of prevailing in showing the subject matter of claim 1 obvious in view of Okuyama alone. We reach a similar conclusion for claims 2, 3, 9–11, 17–20, 26–28, and 34, each of which include these, or similar, limitations.

Petitioner's second theory is that Takahashi discloses the subject matter required by the [1 d] and [1 e] limitations. Pet. 41, 43. As we discussed above, however, Petitioner has not shown sufficiently that Takahashi discloses these limitations, which are required by each challenged claim. Petitioner does not rely on Tsuchida for teaching the subject matter of the [1 d] and [1 e] limitations.

Thus, Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that the subject matter of claims 1–3, 9–11, 17–20, 26–28, and 34 is unpatentable over Okuyama, alone or in combination with Takahashi or Tsuchida.

### *E. Conclusion*

Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that any of the challenged claims are unpatentable under the asserted grounds.

## III.ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied as to all challenged claims of the '861 patent; and

FURTHER ORDERED that no *inter partes* review is instituted.

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