UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD
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SMART MODULAR TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.
_____

Case IPR2014-01374
Patent 8,359,501 B1
_____

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* GAUDETTE.

Opinion Dissenting filed by *Administrative Patent Judge* CLEMENTS.

GAUDETTE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Smart Modular Technologies Inc. ("Petitioner") filed a Petition (Paper 7, Corrected Petition ("Pet.")) on August 23, 2014, requesting institution of an *inter partes* review of claims 1–20 (the "challenged claims") of U.S. Patent No. 8,359,501 B1 (Ex. 1008, "the '501 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 10). Based on these submissions, an *inter partes* review of claims 1, 2, 4–6, 9–11, 14–17, and 20 was instituted on March 10, 2015, pursuant to 35 U.S.C. § 314. Paper 12 ("Dec. on Inst." or "Institution Decision").

After institution, Patent Owner filed a Response (Paper 21, Corrected Response, "PO Resp."), and Petitioner filed a Reply to the Patent Owner Response (Paper 26, "Reply").

Petitioner filed a Motion to Exclude Evidence. Paper 25; *see also* Paper 36 (Patent Owner's Opposition) and Paper 41 (Petitioner's Reply). Patent Owner also filed a Motion to Exclude Evidence (Paper 33; *see also* Paper 38 (Petitioner's Opposition) and Paper 40 (Patent Owner's Reply)) and a Motion to Exclude Portions of Petitioner's Reply (Paper 34; *see also* Paper 39 (Petitioner's Opposition)).

Oral argument was held on November 17, 2015, and a transcript (Paper 42, "Tr.") has been entered into the record.

The Board has jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial.

For the reasons discussed below, we determine Petitioner has not met its burden to prove, by a preponderance of the evidence, that claims 1, 2, 4–

6, 9–11, 14–17, and 20 of the '501 patent are unpatentable. Petitioner's and Patent Owner's Motions to Exclude are dismissed.

A. Related Matters

The '501 patent claims priority as a continuation of U.S. Patent Application No. 12/422,925, now U.S. Patent No. 8,001,434 ("the '434 patent"). Ex. 1008, 1. Petitioner also requested, and we instituted, an *inter partes* review of the '434 patent: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Case IPR2014-01372 (PTAB March 10, 2015) ("IPR-1372"), Paper 13. We denied Petitioner's requests to institute *inter partes* reviews of the '434 patent and the '501 patent in two additional petitions, filed August 23, 2014: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Case IPR2014-01373 (PTAB March 13, 2015), Paper 16, and Case IPR2014-01375 (PTAB March 13, 2015), Paper 12, respectively. Oral argument in IPR2014-01372 was consolidated with the oral argument in the present *inter partes* review. A final decision in IPR2014-01372 is issued concurrently with this final decision.

The '501 patent also is the subject of IPR2014-00971 ("IPR-971"). We entered a final written decision in that case on December 14, 2015, concluding that claims 1–3, 5–8, and 11–20 are unpatentable on the following grounds: claims 1–3, 5–8, 11–14, and 16–20 under 35 U.S.C. § 102(b) based on Averbuj (U.S. Patent Application Publication No. 2005/0257109 A1, issued November 17, 2005); and claims 1–3, 5, and 14–16 under 35 U.S.C. § 103(a) based on Huang (*An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers*, Fourteenth International Conference on VLSI Design 379–384 (2001), IEEE). *Sandisk Corp. v. Netlist, Inc.*, Case IPR2014-00971 (PTAB

December 14, 2015), Paper 34 ("IPR-971 FWD"). Petitioner Sandisk
Corporation has requested rehearing of our determination that it did not meet
its burden to show unpatentability of claims 4, 9, and 10, and our
determination that it failed to show unpatentability of claim 15 as anticipated
by U.S. Patent Application Publication No. 2005/0257109 A1. *Id.*, Paper
35.

B. The '501 Patent (Ex. 1008)

The '501 patent relates to self-testing electronic memory modules.
Ex. 1008, 1:28–29. A block diagram of an exemplary self-testing memory
module is shown in Figure 1 of the '501 patent, reproduced below.
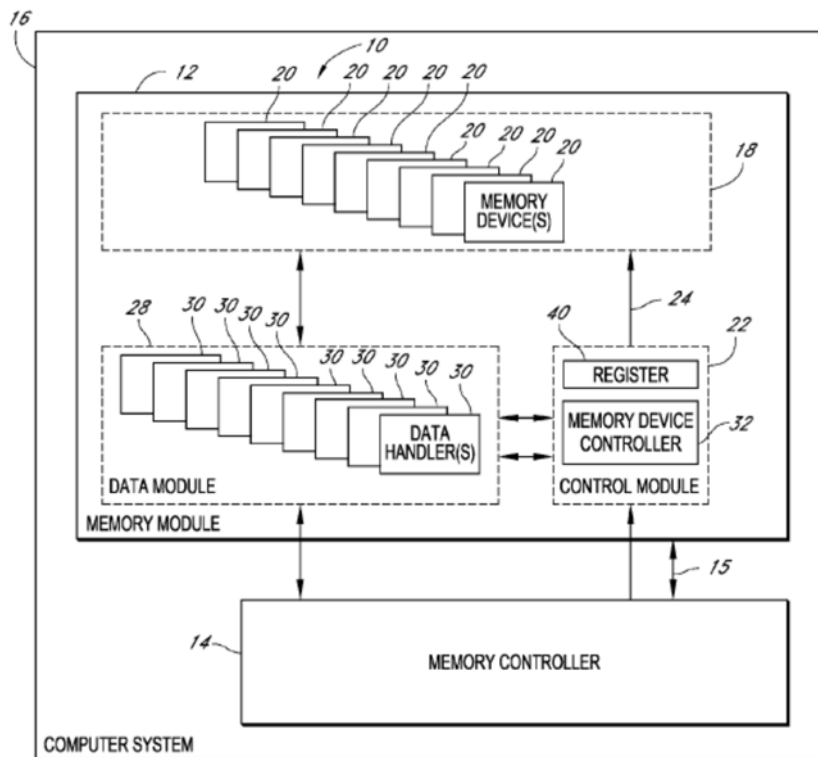
As illustrated in Figure 1, above, "memory module 10 includes a
printed circuit board 12 configured to be operatively coupled to a memory
controller 14 of a computer system 16." *Id.* at 5:6–8. Memory module 10

includes a plurality of memory devices 18, e.g., ETT DRAM chips, each memory device 20 of the plurality of memory devices 18 comprising data, address, and control ports. *Id.* at 3:34–36; 5:10–12.

Memory module 10 further includes data module 28 comprising a plurality of independently operable data handlers 30, and control module 22 that may include a dual input register for registering address and control signals coming from either self-testing logic or from memory controller 14 on the system board. *Id.* at 5:14–16, 42–46. "In various embodiments, the control module 22 includes . . . one or more application-specific integrated circuit[s]" *Id.* at 9:62–64. "[D]ata module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at the normal operating speed of the memory devices 20." *Id.* at 6:5–8. "For example, the data module 28 and/or the control module 22 are configured to provide memory signals (e.g., data, address and control signals) according [to] the operating specification of the memory devices 20." *Id.* at 6:8–11.

"In some embodiments, during testing, the control module 22 generates address and control signals 24 associated with memory locations to be tested and the data module 28 generates corresponding test data patterns and provides them to the appropriate memory devices 20." *Id.* at 5:48–52. "For example, the data module 28 may receive a write command from the control module 22 and provide data to be written to certain locations in the memory devices 20 during a write operation." *Id.* at 5:52–55.

A. Illustrative Claims

Of the challenged claims, claims 1 and 16 are independent, and are reproduced below:

1.   A memory system configured to be operatively coupled to a memory controller of a computer system, the memory system comprising:

a plurality of memory chips;

a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips;

a control circuit configured to generate address and control signals, wherein the memory system is configured to test the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the one or more data handlers.

16.   A method of operating a memory system configured to be operatively coupled to a memory controller of a computer system, the memory system having a plurality of memory chips, the method comprising:

operating a plurality of data handlers independently from one another to generate and transmit data to one or more memory locations of one or more memory chips of the plurality of memory chips;

operating a control circuit to generate address and control signals; and

testing the one or more memory locations of the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the plurality of data handlers.

C. The Instituted Ground of Unpatentability

We instituted the instant *inter partes* review of claims 1, 2, 4–6, 9–11, 14–17, and 20 based on anticipation under 35 U.S.C. § 102(b) by Averbuj, U.S. Patent No. 7,392,442 B2, issued June 24, 2008 (Ex. 1011, "Averbuj"). As indicated in Section I.A., above, in IPR-971, we held claims claims 1–3, 5–8, 11–14, and 16–20 of the '501 patent unpatentable under 35 U.S.C. § 102(b) based on U.S. Patent Application Publication No. 2005/0257109 A1, the published application of the Averbuj patent on which the instituted ground of unpatentability in this proceeding is based.

D. Expert Testimony

Petitioner relies on the testimony of Dr. Nader Bagherzadeh in support of its patentability challenge. Pet. 1. Dr. Bagherzadeh executed a declaration (Ex. 1009, "the Bagherzadeh Declaration") in support of the Petition. Dr. Bagherzadeh was cross-examined on the subject matter of his declaration, and a transcript of the testimony was filed as Exhibit 2012.

Dr. Bagherzadeh testifies as follows: "In 1979 and 1987, respectively, [he] earned a master of science in electrical engineering and a doctorate degree in computer engineering from the University of Texas at Austin." Ex. 1009 ¶ 4. He has been involved in design and development of digital systems for more than 30 years. *Id.* ¶ 6. Dr. Bagherzadeh joined the University of California, Irvine, in 1987, and has "been teaching, researching, and consulting regarding almost all aspects of memory design for high performance computer systems, including but not limited to DRAMs and SRAMs." *Id.* ¶ 7. He has been employed as a professor in the department of Electrical Engineering and Computer Science at the

University of California, Irvine, since 2003. *Id.* ¶ 5. In 2000, Dr. Bagherzadeh became a cofounder of Morpho Technologies, a high tech company focused on the design and development of low power and high performance digital signal processors for mobile applications. *Id.* ¶ 7. He was involved in evaluating patents, technical reports and presentations related to memory chip designs, DSPs, and parallel processing algorithms for mobile platforms. *Id.*

Patent Owner relies on the testimony of Dr. Carl Sechen. PO Resp. 1. Dr. Sechen executed a declaration (Ex. 2019, "the Sechen Declaration") in support of Patent Owner's Response. Dr. Sechen was cross-examined on the subject matter of his declaration, and a transcript of the testimony was filed as Exhibit 1031.

Dr. Sechen testifies as follows: he has an M.S. degree in Electrical Engineering from the Massachusetts Institute of Technology and "was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986." Ex. 2019 ¶ 5. Dr. Sechen has been a Professor of Electrical Engineering for more than 28 years. *Id.* ¶ 2. During this time period, his research has focused on design and computer-aided design of digital integrated circuits, including the design of DRAM, and he has taught numerous students how to design DRAM memories. *Id.* Dr. Sechen has "also been involved in numerous research projects on VLSI design and memory design[, and has] taught numerous graduate researchers how to design digital integrated circuits, including memories." *Id.* ¶ 4.

The parties do not dispute that Dr. Bagherzadeh and Dr. Sechen are qualified to testify as experts under FRE 702.

II. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is relevant to claim construction and anticipation. *See Yorkey v. Diab*, 605 F.3d 1297, 1300 (Fed. Cir. 2010) (explaining that a determination of anticipation involves interpreting the claim language and then comparing the construed claim to a prior art reference); *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259–60 (Fed. Cir. 2010) ("[C]laim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.").

Dr. Bagherzadeh and Dr. Sechen agree that the field of art is "memory module design with features for built-in self-test (BIST)." Ex. 2019 ¶ 21; *see also* Ex. 1009 ¶ 17.

Dr. Bagherzadeh testifies that

> a person of ordinary skill in the art for the '501 patent in April 2008 would have a bachelor's degree or the equivalent training or experience in electrical engineering or computer engineering, and at least one year of experience relating to memory systems and BIST.

> A person having a bachelor's degree or the equivalent training or experience in electrical engineering or computer engineering would have experience with digital circuit design, memories and computer architecture. An additional year of experience relating to memory systems and BIST would focus on those areas and allow one to recognize current issues with respect to the field.

Ex. 1009 ¶¶ 19–20; *see id.* ¶ 16 ("My understanding is that the earliest possible priority date of the '501 patent is April 14, 2008.").

Dr. Sechen testifies that

> one of ordinary skill in the art at the time of filing the application(s) for the '434 [sic, '501] Patent, who would be working on the design of memory devices and memory modules,

would have at least a Bachelor of Science degree in electrical engineering or computer engineering, and at least five years of industry experience designing memory devices and memory modules. Alternatively, one of ordinary skill in the art would have an M.S. degree in electrical engineering or computer engineering, and at least three years of industry experience designing memory devices and memory modules. Moreover, one of ordinary skill in the art would have a Ph.D. degree in electrical engineering or computer engineering, and have at least one year of industry experience designing memory devices and memory modules.

Ex. 2019 ¶ 21.

The difference in the opinions of the two experts is essentially that Dr. Sechen believes a person of ordinary skill in the art would have additional experience, education, or a combination of the two, beyond that proposed by Dr. Bagherzadeh. Both experts have been employed as professors since the mid 1980s. Dr. Bagherzadeh also has some experience working with engineers in the industry by virtue of his employment with AT&T Bell Labs from 1980–1984 (Ex. 1009 ¶ 6; *id.* Appx. A). Both experts were awarded bachelors and masters degrees in electrical engineering. Dr. Bagherzadeh was awarded a doctorate in computer engineering, while Dr. Sechen was awarded a doctorate in electrical engineering.

Based on a comparison of Dr. Bagherzadeh's and Dr. Sechen's declarations (Exs. 1009, 2019), we find Dr. Bagherzadeh has a broader range of educational and work experience, and, therefore, accord greater weight to his opinion as to the level of ordinary skill in the art. Dr. Bagherzadeh's opinion is consistent with our finding as to the level of ordinary skill in the art in our Final Written Decision in IPR-971. We, therefore, adopt our finding in IPR-971 as to the level of ordinary skill in the art:

[A] person of ordinary skill in the art at the time of the '501 patent would have a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.

IPR-971 FWD, 10–11 (noting that our finding was "based on our review of the '501 patent and the types of problems and solutions described in the '501 patent and cited prior art").

III. CLAIM CONSTRUCTION

In its Petition, Petitioner offers specific constructions for the claim terms "operatively coupled," "ports," "to generate," "[operated/operating [. . .] independently," and "cyclic data." Pet. 19–22. We determined that, for purposes of our Institution Decision, only the term "generate" required express construction. Dec. on Inst. 7. We interpreted "generate" as meaning "produce" or "cause." *Id.* at 9.

In its Response, Patent Owner disagrees with our interpretation of "generate" as meaning "cause." PO Resp. 17–18. Patent Owner contends our "Institution Decision also provides a construction for 'configured to generate,'" as recited in claim 1, and proposes its own construction for this phrase. *Id.* at 9 (citing Dec. on Inst. 9). In its Reply, Petitioner asserts that our interpretation of "generate" in the Institution Decision is correct (Reply 1), and offers a proposed construction for the term "configured" (*id.* at 9–10). Patent Owner's and Petitioner's proposed constructions for the disputed claim language are listed in the table below.

Claim Term/Phrase	Patent Owner's Proposed Construction	Petitioner's Proposed Construction
generate	produce (PO Resp. 17)	cause or initiate transmission (Pet. 20–21) produce or cause (Reply 1)
configured to generate	programmed to generate/produce (*see* PO Resp. 9)	arranged or prepared to produce or cause (Reply 9–10)

In support of their proposed constructions of the disputed claim language, the parties rely on language in the '501 patent and extrinsic evidence. *See generally*, Pet. 20–21; PO Resp. 8–33; Reply 1–17. Neither party relies on prosecution history disclaimer in support of its proposed constructions.

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–80 (Fed. Cir. 2015) ("Congress implicitly approved the broadest reasonable interpretation standard in enacting the AIA," and "the standard was properly adopted by PTO regulation."), *cert. granted*, *sub nom. Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 890 (mem.) (2016). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007); *see also Trivascular, Inc. v. Samuels*, No. 2015-1631, 2016 WL 463539, at *3 (Fed. Cir. Feb. 5, 2016) ("Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution

history."). Any special definitions for claim terms must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

"[T]he Board may rely on dictionaries 'so long as the dictionary definition does not contradict any definition found in or ascertained by reading the patent document.'" *Belden Inc. v. Berk-Tek LLC*, 610 Fed. App'x 997, 1002 (Fed. Cir. 2015) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1322–23 (Fed. Cir. 2005)). Expert testimony is useful to explain terms of art, and the state of the art at any given time, but cannot be used to prove "the proper or legal construction of any instrument of writing." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015) (internal citations omitted); *see also* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). A court may revisit and alter its construction of claim terms as the record in a case develops. *See Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd*, 599 F.3d 1308, 1316 (Fed. Cir. 2010).

A. Generate

The terms "generate" and "generated" are used in both independent claims 1 and 16. Petitioner contends "[t]he Institution Decision correctly found that the intrinsic and extrinsic record supported construing 'generate' as 'cause' or 'produce.'" Reply 1. Patent Owner contends "'generate' is properly construed to mean 'produce,'" but "a construction of generate that

includes 'cause' is unsupported by – and contradictory to – the intrinsic and
extrinsic evidence, and fails to provide reasonable clarity." PO Resp. 17–18.
The same respective constructions of "generate" were advanced by Patent
Owner and the petitioner, Sandisk Corporation, in IPR-971. *See* IPR-971
FWD, 23–25.

  We provided an extensive analysis of the term "generate" in our Final
Written Decision in IPR-971. *See id.* at 22–30. "[W]e agree[d] with Patent
Owner that the broadest reasonable interpretation of the claim term
'generate' is 'produce' and that 'generate' does not mean 'cause' or 'cause
to produce.'" *Id.* at 29. We interpreted the claim language "address and
control signals *generated* by the control circuit" (claims 1 and 16) as
"encompassing signals . . . that originated in the control circuit . . . ,
including by transformation or modification of information and/or data
received from another component. *Id.* We also stated that "[w]e [did] not
interpret this language as encompassing signals and data received by the . . .
control circuit from another component, and merely provided, propagated,
sent, or input to memory devices, without transformation or modification by
the control circuit." *Id.* at 29–30.

  In support of its contention that "generate" also should be interpreted
as meaning "cause," Petitioner relies on extrinsic evidence that was not
before us in IPR-971, i.e., the Bagherzadeh Declaration (Ex. 1009) ¶ 28,
ANSI/IEEE 100 - Standard Dictionary of Electrical and Electronic Terms,
Fourth Edition, 1988 (Ex. 1016, "IEEE")), and *Webster's II New College
Dictionary*, 2001 (Ex. 1032, "Webster's II"). *See* Pet. 20–21; Reply 1–9.
We consider this evidence as it is relevant to whether the term "generate"
has a particular meaning to one of ordinary skill in the art. *See Trivascular,*

2016 WL 463539, at *3 ("Construing individual words of a claim without considering the context in which those words appear is simply not 'reasonable.' Instead, it is the 'use of the words in the context of the written description and customarily by those of skill in the relevant art that accurately reflects both the "ordinary" and "customary" meaning of the terms in the claims.'" (quoting *Ferguson Beauregard/Logic Controls, Div. of Dover Res., Inc. v. Mega Sys., LLC*, 350 F.3d 1327, 1338 (Fed. Cir. 2003))).

The IEEE defines "generate (computing systems)" as: "[t]o produce a program by selection of subsets from a set of skeletal coding under the control of parameters." Ex. 1016, 5. Dr. Bagherzadeh cites the IEEE definition in support of his testimony that "[t]he broadest reasonable interpretation of the claim [term] 'to generate' in claims 1 and 16, is 'to cause or initiate transmission.'" Ex. 1009 ¶ 28 (also citing Ex. 1008, 6:3–5, 10:67–11:2, 6:14–17). Dr. Bagherzadeh testifies that "[t]his interpretation is consistent with the specification and extrinsic evidence because they describe generating as initiating or transmitting, which is also the broadest interpretation of 'generate.'" *Id.*

We are not persuaded by Dr. Bagherzadeh's testimony because it is devoid of specific facts and analysis as to what led him to conclude that a person of ordinary skill in the art would interpret the claim term "generate" in the manner Petitioner proposes. *See id.* Dr. Bagherzadeh does not explain how the IEEE definition supports an interpretation of generate as "cause or initiate transmission," terms that do not appear in the IEEE definition. *See id.* Nor does Dr. Bagherzadeh identify other extrinsic evidence which he believes to be consistent with an interpretation of

"generate" as meaning "cause or initiate transmission." *See id.* Likewise, Dr. Bagherzadeh has not explained why he believes the '501 patent "describe[s] generating as initiating or transmitting" (Ex. 1009 ¶ 28), as these terms do not appear in the cited portions of the '501 patent. *See* Ex. 1008, 6:8–10, 11:4–11:6, 6:19–22.[1] Accordingly, Dr. Bagherzadeh's testimony does not persuade us to accept Petitioner's interpretation of "generate" as meaning "cause."

Petitioner contends "Dr. Bagherzadeh's use of the IEEE definition specifically illustrates that 'generate' includes 'selection . . . from a set,' which implies that 'generate' must <u>not be limited to creating</u> from previously undefined values, which may be a more traditional meaning, but holds little value in the intrinsic evidence in this proceeding." Reply 6. Petitioner has not identified corresponding testimony by Dr. Bagherzadeh or other evidentiary support for this statement and, therefore, this argument is

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[1] We understand Dr. Bagherzadeh's citations to "6:3–5, 10:67–11:2, 6:14–17" to be a typographical mistake. In IPR-1372, Dr. Bagherzadeh cites to the same column and line numbers in the '434 patent in support of an interpretation of the claim term "generate" as meaning "cause or initiate transmission." *See* IPR-1372, Ex. 1009 ¶ 28. The disclosures at the cited column and line numbers differ in the '434 and '501 patents. Based on the citations to the '501 patent relied upon by Petitioner (*see* Pet. 20–21), we presume Dr. Bagherzadeh intended to rely on column 6, lines 8–10 and 19–22, and column 11, lines 4–6 of the '501 patent, which disclosure is identical to column 6, lines 3–5 and 14–17, and column 10, line 67–column 11, line 2 of the '434 patent. *Compare* Ex. 1008, 6:8–10, 11:4–6, 6:19–22 *with* IPR-1372, Ex. 1008 (the '434 patent), 6:3–5, 10:67–11:2, 6:14–17. This disclosure, like the disclosure in the '501 patent cited in paragraph 28 of Dr. Bagherzadeh's declaration, does not include the terms "initiating or transmitting."

likewise unpersuasive. *See id.*

In support of its construction of "generate" as meaning "cause," Petitioner also relies on a finding in our Institution Decision that such construction is supported by Merriam-Webster's Collegiate Dictionary, wherein one definition of "generate" is "to be the cause of" (Ex. 2009, 3). Reply 2 (citing Dec. on Inst. 9 [sic, 8]). This argument is not persuasive because the definition in Merriam-Webster's Collegiate Dictionary contradicts the definition of "generate" that we ascertained upon reading the '501 patent as discussed in our Final Written Decision in IPR-971. *See Belden*, 610 Fed. App'x at 1002.

In sum, we are not persuaded that Petitioner's extrinsic evidence supports a finding that a customary meaning of "generate" to one of ordinary skill in the art is "cause."[2] We, therefore, determine the broadest reasonable construction of "generate" is "produce" for the reasons stated above and in our Final Written Decision in IPR-971. We adopt and incorporate by reference our analysis and construction of the term "generate" in our Final Written Decision in IPR-971 (IPR-971 FWD, 22–30).

B. Configured to

The term "configured to" is used in independent claim 1, but not in independent claim 16. In our Final Decision in IPR-971, we construed "configured to" as "designed to, adapted to, or arranged to." *See* IPR-971 FWD, 18–22. Petitioner contends "configured" should be construed as

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[2] Petitioner relies on *Webster's II*, for a definition of "cause." *See* Reply 4, 6–8 (citing Ex. 1032, 3). Having determined the broadest reasonable interpretation of "generate" does not encompass "cause," we do not find this evidence relevant to our claim construction analysis.

"arranged" or "prepared." Reply 9–10. Responsive to this Board panel's questioning during the oral hearing, however, Petitioner agreed that "designed to, adapted to, or arranged to" was an acceptable definition for the claim term "configured to." *See* Tr. 22:7–17.

Patent Owner contends the phrase "configured to generate" should be construed as "programmed to generate." PO Resp. 9. Patent Owner does not propose a separate construction for the term "configured." *See generally id.* at 9–17. In support of its proposed construction, Patent Owner relies on language in the '501 patent and the testimony of its expert, Dr. Sechen. *See id.* Dr. Sechen testifies as to the meaning of "configured to generate," but does not provide a separate discussion of the meaning of "configured to" outside the context of "configured to generate." *See* Ex. 2019 ¶¶ 42–57.

As explained in our Final Decision in IPR-971, the term "configured to" is used in the '501 patent in conjunction with numerous terms, such as "provide" and "selectively input," and there is a presumption that the term "configured to" should carry the same meaning in each instance. *See* IPR-971 FWD, 18–19. The evidence relied on by Patent Owner in support of its proposed construction of the term "configured to" in the present *inter partes* review does not differ materially from the evidence relied upon by Patent Owner in IPR-971. *Compare* PO Resp. 9–17 *with* IPR-971, Paper 19, 14–19. Accordingly, we determine the broadest reasonable construction of "configured to" is "designed to, adapted to, or arranged to" for the reasons stated above and in our Final Written Decision in IPR-971. We adopt and incorporate by reference our analysis and construction of the term "configured to" in our Final Written Decision in IPR-971 (IPR-971 FWD, 18–22).

In summary, we construe the claim terms in controversy as follows:

Claim Term/Phrase	Interpretation
Generate	Produce
Configured to	Designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]
Configured to Generate	Designed, adapted, or arranged to produce

IV. ALLEGED ANTICIPATION OF CLAIMS 1, 2, 4–6, 9–11, 14–17, and 20 BY AVERBUJ

A. Principles of Law

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

> A single prior art reference that discloses, either expressly
> or inherently, each limitation of a claim invalidates that claim by
> anticipation. Thus, a prior art reference without express
> reference to a claim limitation may nonetheless anticipate by
> inherency. "Under the principles of inherency, if the prior art
> necessarily functions in accordance with, or includes, the claims
> limitations, it anticipates."

Perricone v. Medicis Pharm. Corp., 432 F.3d 1368, 1375–76 (Fed. Cir.

2005) (citations omitted). "In general, a limitation or the entire invention is inherent and in the public domain if it is the 'natural result flowing from' the explicit disclosure of the prior art." *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003).

"[T]he Board is not bound by any findings made in its Institution Decision. . . . The Board is free to change its view of the merits after further development of the record, and *should do so* if convinced its initial inclinations were wrong." *Trivascular*, 2016 WL 463539, at *9.

We analyze the instituted ground of unpatentability in accordance with the above-stated principles.

B. Averbuj (Ex. 1011)

Averbuj describes a hierarchical built-in self-test (BIST) architecture wherein a BIST controller provides centralized, high level control of the testing of one or more memory modules. Ex. 1011, 1:64–65, 2:3–4. Figure 1 of Averbuj is reproduced below.
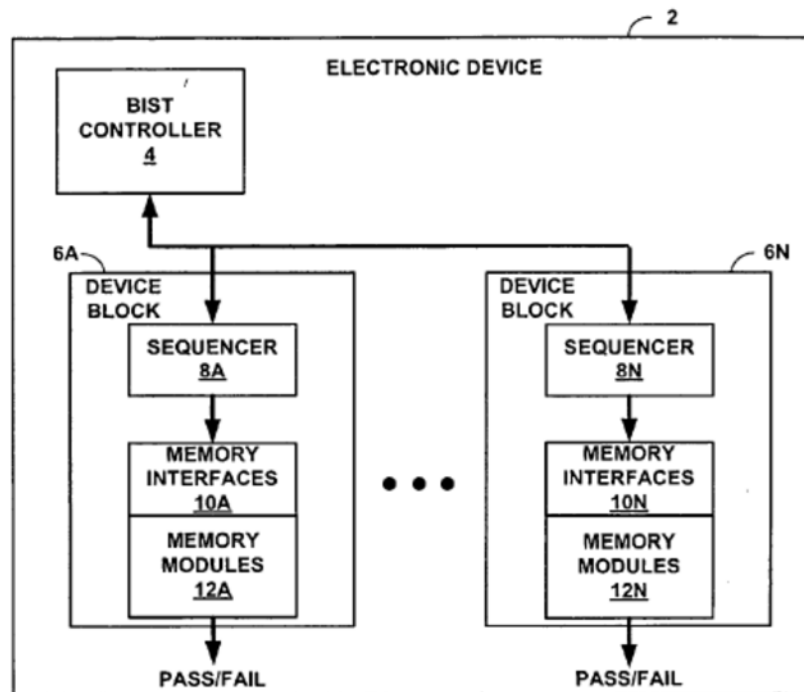
Averbuj Figure 1, above, "is a block diagram illustrating an example electronic device 2 having a distributed, hierarchical built-in self-test (BIST) architecture." *Id.* at 3:62–64. "[E]lectronic device 2 includes a built-in self-test (BIST) controller 4 that provides centralized, high-level control over testing of device blocks 6A through 6N (collectively 'device blocks 6')." *Id.* at 3:64–67. "Each of device blocks 6 includes a sequencer 8, and a set of one or more memory interfaces 10 and one or more respective memory modules 12." *Id.* at 3:67–4:3.

BIST controller 4 is illustrated in Figure 2, reproduced below.
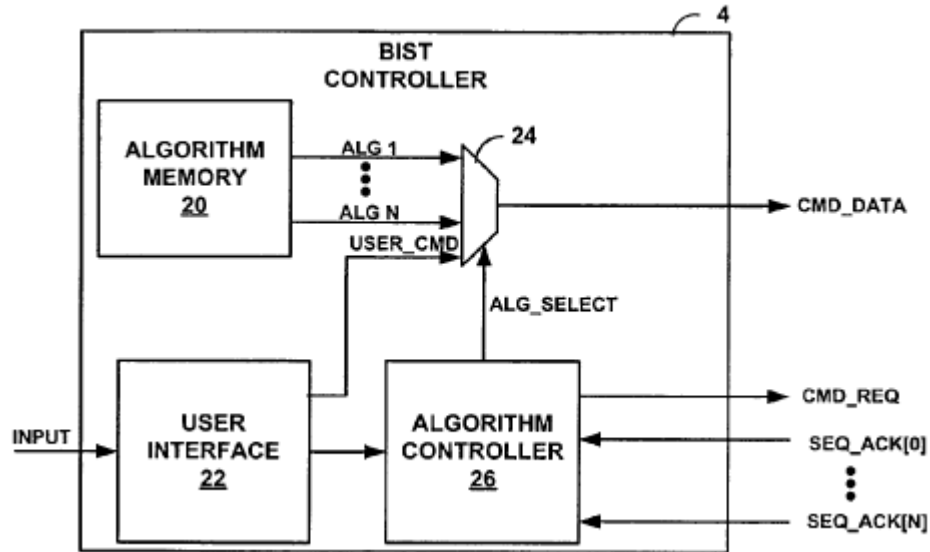
Averbuj Figure 2, above, "is a block diagram illustrating an example

embodiment of a BIST controller." *Id.* at 3:39–40. BIST controller 4

includes algorithm controller 26 that can be invoked either by a user through

user interface 22 or automatically upon power-up of electronic device 2. *Id.*

at 5:12–16. "Once invoked, algorithm controller 26 provides an algorithm

select signal (ALG_SELECT) to multiplexer 24 to select one of the

algorithms stored within algorithm memory 20." *Id.* at 5:16–19.

Alternatively, user interface 22 may programmably receive algorithms

via external input, and deliver the received algorithms to multiplexer 24. *Id.*

at 5:41–43. The algorithms, whether stored in algorithm memory 20 or

received via external input, have a similar form, i.e., "a sequence of binary

commands in which each command defines a test within the overall

algorithm." *Id.* at 5:43–47. BIST controller 4 provides and communicates

the selected algorithm to sequencers 8 for application to device blocks 6 as a

stream of binary commands (CMD_DATA), "each command specif[ying] an

operational code [(OP CODE)] and a set of parameters that define one or

more memory operations without regard to the physical characteristics or timing requirements of memory modules 12." *Id.* at 4:4–12, 5:19–21.

Figure 8, reproduced below, "is a block diagram illustrating an example data structure of a command issued by BIST controller 4." *Id.* at 9:15–16.
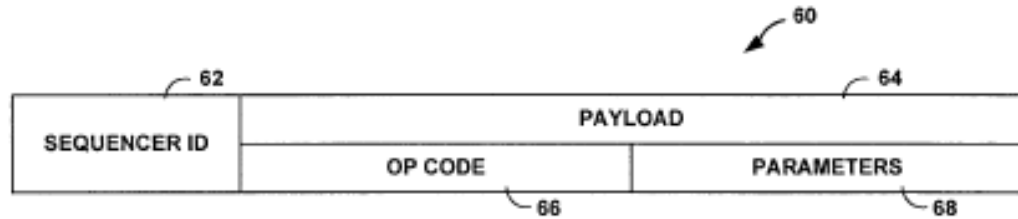
In the embodiment shown in Figure 8, above, "command 60 includes a sequencer identifier (ID) 62, and a payload 64. Sequencer ID 62 identifies a sequencer, e.g., sequencer 8A, to which command 60 is being issued." *Id.* at 9:17–20. "Payload 64 of command 60 carries binary data that defines the command itself. In particular, payload 64 includes an operational code (OP CODE) 66 and a set of parameters 68." *Id.* at 9:29–31. In one embodiment, for example, "OP CODE 66 and parameters 68 comprise three bits and twenty-nine bits, respectively, to form a 32-bit command." *Id.* at 9:58–60. "OP CODE 66 specifies a particular function to be performed by the receiving sequencers 8." *Id.* at 9:32–33. An exemplary OP CODE is SET ADDRESS (OP CODE 100), which "[s]ets a specific starting address as well as a maximum address limit for a test algorithm as applied to the memory modules." *Id.* at Table 1.

Figure 5, below, illustrates an exemplary sequencer 8A. *Id.* at 3:46–47.
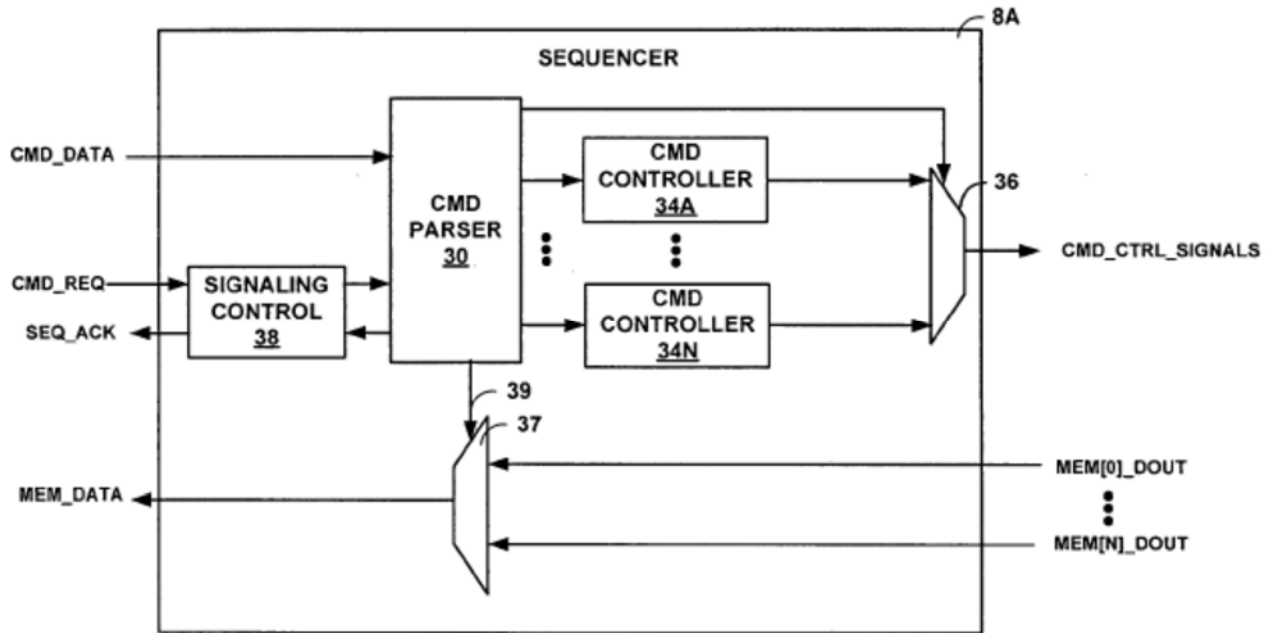
As shown in Figure 5, above, exemplary sequencer 8A includes command parser 30 that receives command data (CMD_DATA) from BIST controller 4. *Id.* at 6:24–26. Command parser 30 processes the commands from BIST controller 4 to identify a specified operation, e.g., by identifying an OP CODE specified by the command. *Id.* at 6:26–29. Based on the specified operation, command parser 30 may extract one or more parameters from the command, and pass the extracted parameters to a selected command controller (i.e., one of command controllers 34A-34N). *Id.* at 6:30–37. The invoked command controller, in turn, issues a sequence of one or more operations to each memory interface 10, sequentially driving the appropriate command control signals (CMD_CTRL_SIGNALS) to carry out each operation of the sequence. *Id.* at 6:41–43. "Memory interfaces 10 handle specific interface requirements for each of memory modules 12. For example, each of memory interfaces 10 may be designed in accordance with

the particular signal interface requirements and physical characteristics of the respective one of memory modules 12." *Id.* at 4:45–49.

C. Arguments

Independent claims 1 and 16 recite, respectively, "[a] memory system" and "[a] method of operating a memory system." Both claims recite "a plurality of memory chips" and "a plurality of data handlers." Petitioner contends the claimed "memory chips" read on Averbuj's memory modules 12 and the claimed "data handlers" read on the combination of sequencers 8 and memory interfaces 10. Pet. 23. Independent claim 1 further recites "a control circuit *configured to generate address and control signals*, wherein the memory system is configured to test the one or more memory chips using the *address and control signals generated by the control circuit*." Ex. 1008, claim 1 (emphasis added). Independent claim 16 recites steps of "operating a *control circuit to generate address and control signals*" and "testing the one or more memory locations of the one or more memory chips using the *address and control signals generated by the control circuit*." *Id.*, claim 16 (emphasis added). With respect to the above-quoted limitations relating to generating/generated address and control signals, the Petition states:

> the BIST controller 4 of Averbuj '442 represents circuitry of a control circuit that provides the *SET ADDRESS* and *CMD_REQ* signals as *OP CODE* for testing the memory components 12A-N. Ex. 1011, Fig. 2 and Column 9: Table 1. The SET ADDRESS and CMD_REQ signals include address and control signals for the testing functions. Since the BIST controller 4 provides the *SET ADDRESS* and *CMD_REQ* signals as *OP CODE*, a POSITA [("person of ordinary skill in the art")] would understand that the BIST controller 4 is programmable to provide address and

control signals as recited in part by the Challenged Claims. Ex.
1009, Bagherzadeh Decl., ¶ 33.

Pet. 24.

Patent Owner argues Averbuj's BIST controller 4 does not "generate"
the OP CODE communicated to sequencers 8, and Petitioner has not met its
burden to show that Averbuj's BIST controller 4 is "configured to generate"
(claim 1) or can be "operat[ed] . . . to generate" (claim 16) address signals
for testing the memory chips in the manner recited in claims 1 and 16 of the
'501 patent. PO Resp. 45–46. As discussed in greater detail below, we find
this argument persuasive, and, for this reason, conclude Petitioner failed to
meet its burden to prove unpatentability of claims 1, 2, 4–6, 9–11, 14–17,
and 20 of the '501 patent.[3]

D. Expert Testimony

In support of its argument that Averbuj's BIST controller 4 is not
"configured to generate" (claim 1) and cannot be "operat[ed] . . . to
generate" (claim 16) address signals, Patent Owner relies on paragraphs
133–141 of the Sechen Declaration. *See id.* at 45–49. Patent Owner also
relies on Dr. Bagherzadeh's cross-examination testimony (*id.* at 46–47
(quoting Ex. 2012, 55:6–56:9)) regarding Averbuj Figure 2 (*see* Ex. 2012,
53:4–5; *see generally id.* at 53:4–56:9).

With reference to Averbuj Figure 2 (*see* Section IV.B., above,
wherein this figure is reproduced and described), Dr. Bagherzadeh testifies
that OP CODE residing in the algorithm memory of BIST controller 4 are

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[3] Because we are persuaded by this argument that Petitioner has not met its
burden to show unpatentability, we find it unnecessary to address the
additional arguments advanced by Patent Owner in its Response.

generated by hand or by a tool (Ex. 2012, 55:20–56:9), and he identifies a

compiler as a tool for generating such code (*id.* at 30:23–24, 41:1–4; *see id.*

at 55:6–25).[4] Dr. Bagherzadeh testifies that a compiler is not illustrated in

Averbuj Figure 2, and that he did not recall any mention of the word

"compiler" in Averbuj. *See* Ex. 2012, 54:8–55:5. Dr. Bagherzadeh further

testifies that "99 percent of the designs or chips do not have a compiler on-

board." *Id.* at 54:21–22. Dr. Bagherzadeh testifies that Averbuj Figure 2,

without consideration of any other disclosure in Averbuj, illustrates that a

multiplexer selects an input from the algorithm memory and "the output []

reflect[s] what's in the input, based on the selection." *Id.* at 54:8–13. Dr.

Bagherzadeh testifies that assuming "no other hardware components

between . . . [CMD_DATA] and the input," CMD_DATA is stored in the

algorithm memory. *Id.* at 54:15–19.

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[4] Petitioner contends "[t]he discussion of a compiler, from PO's deposition
of [Dr. Bagherzadeh], was hypothetical and specific to an article coauthored
by [Dr. Bagherzadeh]." Reply 22 (citing Ex. 2012, 15:2–19:3).[4] We were
unable to locate a discussion of a compiler or any reference to an article
coauthored by Dr. Bagherzadeh in the cited portions of Dr. Bagherzadeh's
deposition transcript. Dr. Bagherzadeh's first discussion of a compiler
appears to be in connection with a use thereof in MorphoSys (*see* Ex. 2012,
30:12–20), a chip fabricated by Morpho Technologies (*id.* at 19:2–9), a
company co-founded by Dr. Bagherzadeh (Ex. 1009 ¶ 7). An article relating
to MorphoSys and co-authored by Dr. Bagherzadeh (*see* Ex. 2014,
"MorphoSys: Case Study of A Reconfigurable Computing System
Targeting Multimedia Applications") is introduced on page 39 of the
deposition transcript. *See* Ex. 2012, 39:19–22, cited in PO Resp. 25. In any
event, Petitioner's argument is not persuasive because we find the testimony
on pages 54–56 of the Bagherzadeh transcript supports Patent Owner's
argument. *See* Section IV.E. *infra*.

Dr. Sechen testifies that

> the Petition fails to identify every element of claims 1, 20, and 29 [sic, 1 and 16] for at least two reasons[:] (1) because the CMD_REQ and SET ADDRESS are not generated ("produced" or "caused") by the purported control module (Averbuj's BIST controller 4), and [(2)] because the OP CODE is not generated ("produced" or "caused") by the alleged control module (Averbuj's BIST controller 4).

Ex. 2019 ¶ 136. Dr. Sechen testifies, more specifically, that the Petition fails to explain how Averbuj's BIST controller 4 "generate[s]/produce[s] OP CODE," "because the Petition does not state that Averbuj's BIST Controller includes a compiler, as described by Dr. Bagherzadeh." *Id.* ¶ 138. Dr. Sechen testifies that "[b]ecause SET ADDRESS (OP CODE 100) is a predefined 3-bit sequence, . . . it is not 'generated' by Averbuj's BIST Controller." *Id.* ¶ 140. Dr. Sechen further testifies that "command 60, which carries the OP CODE [] (*e.g.* SET ADDRESS), . . . is not 'generated' by Averbuj's BIST Controller," but "is merely stored in memory and is output as part of 'a stream of binary commands.' (Ex. 1011 at 5:1–21.)" Ex. 2019 ¶ 141.

E. Analysis

After considering the parties' arguments and evidence, we determine Petitioner has not shown, by a preponderance of the evidence, that Averbuj discloses a control circuit that is "configured to generate" (claim 1) or can be "operat[ed] . . . to generate" (claim 16) address signals for testing the memory chips in the manner recited in claims 1 and 16 of the '501 patent.

As noted in Section III, above, in its Petition, Petitioner proposes construing the claim term "generate" as "cause or initiate transmission" (Pet. 20–21). The Petition cites the following disclosure in the '501 patent in

support of this construction: "'the data module 28 and/or the control circuit
22 are **<u>configured to provide</u>** memory signals (e.g., data, address and
control signals)' Ex. 1008, '501 patent, 6:8-10 (emphasis added)." Pet. 20.
The Petition states that Averbuj teaches "a control circuit configured to
generate" (claim 1) and "operating a control circuit to generate" (claim 16)
address signals for testing the memory chips as recited in claims 1 and 16,
because Averbuj's "BIST controller 4 is programmable *to provide* address
and control signals." Pet. 24 (emphasis added); *see* PO Resp. 49–50.

For purposes of our Institution Decision, we interpreted "generate" as
used in the '501 patent claims as meaning "cause" or "produce." *See* Dec.
on Inst. 9. As indicated in Section III.A., above, subsequent to that decision
and the oral hearing in the present *inter partes* review, we again considered
the meaning of the claim term "generate" in our final decision in IPR-971,
and determined that the broadest reasonable interpretation of the '501 patent
claim term "generate" is "produce," and that "generate" does not mean
"cause" or "cause to produce." *See* IPR-971 FWD, 22–30. In Section III.A.,
above, we considered extrinsic evidence in support of Petitioner's
interpretation of "generate" as meaning "cause" that was not before us in
IPR-971, but concluded the broadest reasonable interpretation of "generate"
is "produce." We, therefore, adopted and incorporated by reference in the
present final decision our analysis and construction of the terms "generate"
and "configured to generate" in our Final Written Decision in IPR-971. *See*
Section III., above.

In construing the claim term "generate" in our final decision in IPR-
971, we found that the terms "provide" and "generate" are used in the '501
patent to describe different embodiments of the control circuit, and

determined the claim term "generate" did not mean "provide." *See* IPR-971 FWD, 25–28. We also determined that the phrase "address and control signals generated by the control circuit" (claims 1 and 16) encompasses signals that originated in the control circuit, including by transformation or modification of information received from another component. IPR-971 FWD, 29. We further determined the broadest reasonable interpretation of this claim language does not encompass "signals . . . received by the control circuit . . . from another component, and merely provided, propagated, sent, or input to memory devices, without transformation or modification by the control circuit." *Id.* at 29–30. We stated that "generate," as used in the '501 patent, does not encompass the selection function of a multiplexer. *Id.* at 27.

Petitioner's contention that Averbuj teaches "a control circuit configured to generate address . . . signals" (claim 1) and "operating a control circuit to generate address . . . signals" (claim 16) for testing memory chips, as recited in independent claims 1 and 16, is based on an interpretation of "generate" as meaning "cause." Pet. 20, 24; *see also*, Reply 20–21 (asserting that Averbuj discloses the above-quoted limitations because "the BIST controller of Averbuj *causes* the CMD_REQ and SET ADDRESS signals, representing the claimed 'address and controls signals'" (emphasis added)) (citing Dec. on Inst. 15–16). Petitioner has not explained sufficiently, however, how Averbuj's BIST controller 4 is "configured to generate" (i.e., designed, adapted, or arranged to produce) or "operat[ed] . . . to generate" (i.e., operated to produce) address signals as recited in independent claims 1 and 16, respectively.[5]

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[5] During oral argument, Judge Clements asked Mr. Heafey, counsel for

Moreover, the evidence in this proceeding fails to support a finding that Averbuj's BIST controller 4 generates address signals for testing the memory devices in the manner claimed.

In Averbuj, the algorithms (i.e., CMD_DATA containing OP CODE such as SET ADDRESS (*see* Ex. 1011, 4:4–12, 5:19–21, Table 1)) communicated to sequencers 8 are either received by user interface 22 via external input (*id.* at 5:41–43) or generated by another component (i.e., a component that is not part of BIST controller 4 circuitry) and stored in algorithm memory 20 (*see* Ex. 2012, 30:23–24, 41:1–4, 54:21–22, 55:6–25, 55:20–56:9 (wherein Dr. Bagherzadeh testifies that OP CODE residing in the algorithm memory of BIST controller 4 are generated by hand or by a tool, e.g., a compiler, and that "99 percent of the designs or chips do not have a compiler on-board")). Multiplexer 24 *selects* one of the algorithms (i.e., CMD_DATA) and BIST controller 4 *provides* to sequencers 8 the same CMD_DATA (e.g., address signals) without transformation or modification. *See* Ex. 1011, 4:4–12, 5:16–21; Ex. 2012, 54:8–13 ("Averbuj Figure 2, without consideration of any other disclosure in Averbuj, illustrates that a multiplexer selects an input from the algorithm memory and the output [] reflect[s] what's in the input, based on the selection."). Based on our

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Petitioner, the following question: "Assuming we adopt 'to produce' as the proper construction [of 'to generate'], are [CMD]_REQ and SET ADDRESS produced by BIST controller 4?" Tr. 78:16–18. In response, Mr. Heafey stated: "[T]hose signals are definitely produced by BIST controller 4, yes, they are." *Id.* at 78:19–20. Mr. Heafey did not elaborate, however, nor did he otherwise explain clearly during oral argument how Averbuj's BIST controller 4 is designed, adapted, or arranged to produce address signals for testing the memory devices.

interpretation of the term "generate," as discussed above, an "address . . . signal[] generated by the control circuit," as recited in claims 1 and 16, does not encompass Averbuj's SET ADDRESS signal, because it is produced by a component external to BIST controller 4, and merely selected by multiplexer 24 and provided to sequencers 8 without transformation or modification by BIST controller 4.

In sum, after considering the parties' arguments and evidence, we determine Petitioner has not shown, by a preponderance of the evidence, that Averbuj discloses "a control circuit configured to generate address . . . signals" (claim 1) and "operating a control circuit to generate address . . . signals" (claim 16) for testing memory chips in the manner recited in independent claims 1 and 16. Petitioner does not correct this deficiency in its challenges as to dependent claims 2, 4–6, 9–11, 14, 15, 17, and 20. *See* Pet. 26–34; 35 U.S.C. § 112, ¶ 4 ("A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers."). Because Petitioner has not identified in Averbuj a teaching of each and every limitation recited in claims 1, 2, 4–6, 9–11, 14–17, and 20, Petitioner has not met its burden to show these claims are unpatentable under 35 U.S.C. § 102(b) as anticipated by Averbuj.

V. MOTIONS TO EXCLUDE

Both Patent Owner and Petitioner filed Motions to Exclude.

A. *Petitioner's Motion to Exclude*

Petitioner moves to exclude Exhibit 2018 (the Deposition Transcript of Dr. Donald Alpert) and to strike Section IV(B)(5)(a) of Patent Owner's Response, wherein Patent Owner quotes Dr. Alpert's deposition testimony in

support of its proposed construction of the claim term "generate" (*see* PO
Resp. 31–32). Paper 25, 2. Petitioner argues Dr. Alpert is Sandisk
Corporation's expert in IPR-971 and that Petitioner was not provided notice
or otherwise invited to attend Dr. Alpert's deposition. *Id.* at 3. Petitioner
contends Dr. Alpert's statements are not admissible as evidence in this
proceeding "because they are hearsay and will unfairly prejudice Petitioner."
Id. at 2.

In construing the claim term "generate" in Section III.A., above, we
adopted and incorporated by reference our analysis and construction of this
term on pages 22–30 of our Final Written Decision in IPR-971. In our claim
construction in IPR-971, we considered Dr. Alpert's deposition and
declaration testimony, but did not quote or cite to the testimony relied on by
Patent Owner in Section IV(B)(5)(a) of its Patent Owner Response in the
present proceeding. *Compare* IPR-971 FWD, 23–24 *with* PO Resp. 31–32.
In IPR-971, we determined Dr. Alpert's testimony that one of ordinary skill
in the art would understand the claim term "generate" as meaning "cause" or
"produce" was inconsistent with the '501 patent's implicit definition of this
term as meaning only "produce." *See* IPR-971 FWD, 27 n.4. We, therefore,
did not rely on Dr. Alpert's testimony in our construction of the claim term
"generate" in IPR-971, or in the present case. *See id.*; *see also id.* at 32
("Having considered the ordinary meaning of the term 'generate' in the
context of both the claims and the '501 patent as a whole, we agree with
Patent Owner that the broadest reasonable interpretation of the claim term
'generate' is 'produce,' and that 'generate' does not mean 'cause' or 'cause
to produce.'").

Because we did not rely on Exhibit 2018 or consider the argument in Section IV(B)(5)(a) of Patent Owner's Response in rendering our decision in this proceeding, we dismiss Petitioner's Motion to Exclude Exhibit 2018 and to strike Section IV(B)(5)(a) as moot.

B. Patent Owner's Motions to Exclude

Patent Owner filed a Motion to Exclude "Exhibits 1026, 1029, 1030, and 1032 (or portions thereof)" and requests that we strike the corresponding citations to these exhibits in Petitioner's Reply. Paper 33, 2. We did not rely on these exhibits in rendering our decision. Accordingly, Patent Owner's Motion to Exclude these exhibits is dismissed as moot.

Patent Owner also filed a Motion to Exclude Portions of Petitioner's Reply, contending "Petitioner's Reply improperly presents new theories, never raised in its Petition or adopted by the Board's Institution Order, violating 37 CFR 42.22-23 and applicable law." Paper 34, 1. Patent Owner provides a table identifying the alleged new theories advanced by Petitioner in its Reply (*id.* at 2) and identifies by page and line number specific portions of sections II.A.3, II.B.1.a, II.B.5 & III.B.2 of the Reply that it contends should be excluded as advancing new theories (*see id.* at 2–8).

Our decision is not based on any of the alleged new theories identified by Patent Owner, and Patent Owner does not cite to any of the specific language in the Reply that Patent Owner contends should be excluded. Accordingly, Petitioner's Motion to Exclude portions of Petitioner's Reply is dismissed as moot.

VI.   CONCLUSION

Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 4–6, 9–11, 14–17, and 20 of the '501 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by Averbuj (U.S. Patent No. 7,392,442 B2).

VII.   ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 2, 4–6, 9–11, 14–17, and 20 of U.S. Patent No. 8,359,501 B1 are not held unpatentable under 35 U.S.C. § 102(b) as anticipated by Averbuj (U.S. Patent No. 7,392,442 B2);

FURTHER ORDERED that Petitioner's Motion to Exclude Exhibit 2018 and to strike Section IV(B)(5)(a) of Patent Owner's Response is *dismissed*;

FURTHER ORDERED that Patent Owner's Motion to Exhibits 1026, 1029, 1030, and 1032 to strike the corresponding citations to these exhibits in Petitioner's Reply is *dismissed*;

 FURTHER ORDERED that Patent Owner's Motion to Exclude Portions of Petitioner's Reply is *dismissed*; and

FURTHER ORDERED that, because this is a final decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2014-01374
Patent 8,359,501 B1

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UNITED STATES PATENT AND TRADEMARK OFFICE
_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD
_____

SMART MODULAR TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.
_____

Case IPR2014-01374
Patent 8,359,501 B1
_____

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*, dissenting.

While I agree with the majority's construction of "generate" to mean "produce," I respectfully dissent from the majority's determination that "Petitioner has not explained sufficiently, however, how Averbuj's BIST controller 4 is 'configured to generate' (i.e., designed, adapted, or arranged to produce) or 'operat[ed] . . . to generate' (i.e., operated to produce) address signals as recited in independent claims 1 and 16, respectively." Majority Opinion ("Maj. Op.") 30–31. Although Petitioner's arguments are based on a construction of "generate" that includes cause, and we have construed

"generate" to mean "produce," I believe the evidence cited by Petitioner nevertheless establishes sufficiently that BIST controller 4—identified by Petitioner as the recited "control circuit"—"produces" address signals.

The majority opinion finds that "[i]n Averbuj, the algorithms (i.e., CMD_DATA containing OP CODE such as SET ADDRESS) communicated to sequencers 8 are either received by user interface 22 via external input or generated by another component (i.e., a component that is not part of BIST controller 4 circuitry) and stored in algorithm memory 20." Maj. Op. 31 (citations omitted). As support for its finding that the algorithms are generated by another component, the majority cites the cross-examination of Petitioner's expert, Dr. Bagherzadeh, in which he identifies a person or tool as possible ways of generating the OP CODEs stored in algorithm memory 26:

> Q   Would a compiler be required to generate the op codes?
>
> [Objection]
>
> THE WITNESS: Which op codes?
>
> BY MR. BRADLEY:
>
> Q   The op codes stored in algorithm memory?
>
> A   Required, no.
>
> Q   In what other way could code be generated for algorithm memory?
>
> A   By hand, as I explained to you.
>
> Q   Are there any other ways of generating the code?
>
> [Objection]
>
> THE WITNESS: Those codes that are residing in the memory, right, that's all that we're talking about?

BY MR. BRADLEY:

Q   Right.

A   So either you do it by hand or you have a tool do it.

Q   Okay.

A   There's no – we're talking about code, not the generation of the -- or signals that are generated, just the bits in the code?

Q   The generation of the op codes, yes.

A   Yes. They have to be stored in the memory. Somebody did it by hand, wrote the code, or by a tool.

Q   Okay.

A   There's no other way around it.

Ex. 2012, 54:20–56:9.

The majority appears to understand this testimony by Dr. Bagherzadeh as a description of how BIST controller 4 works *in operation*. I understand this testimony, however, to explain only how the data stored in algorithm memory 26 could have been created and stored in algorithm memory 26 *in the first instance*. At no point in this testimony does Dr. Bagherzadeh suggest that a compiler plays any role during *operation* of BIST controller 4. Indeed, that would be inconsistent with Averbuj's explicit disclosure.

Averbuj explains that the *only* input received by BIST controller 4 is an invocation of some sort, whether an "external input, such as a control signal from an external testing apparatus" or an automatic invocation, and, as a result of that input, CMD_DATA, among other signals, is output:

> User interface 22 invokes algorithm controller 26 in response to external input, such as a control signal from an external testing

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apparatus. Alternatively, algorithm controller may be automatically invoked upon power-up of electronic device 2. Once invoked, algorithm controller 26 provides an algorithm select signal (ALG_SELECT) to multiplexer 24 to select one of the algorithms stored within algorithm memory 20. Once selected, a stream of binary commands that comprises the selected algorithm is applied to device blocks 6 as command data (CMD_DATA).

Ex. 1011, 5:12–21. Thus, in this embodiment, a control signal goes into BIST controller 4 and CMD_DATA, *inter alia*, comes out of BIST controller 4. In this embodiment, BIST controller 4 does not propagate signals through to its ouput because it does not receive CMD_DATA at user interface 22. For that reason, I find that BIST controller 4 "produces" CMD_DATA, including, *inter alia*, SET ADDRESS, which Petitioner identifies as the recited "address . . . signal[]" (Pet. 24).

The fact that the data output by BIST controller 4—i.e., CMD_DATA—is read from a memory within BIST controller 4 so that it can subsequently be output goes to *how* BIST controller 4 "produces" that data. It does not show that the data is "produced" by another component. Moreover, the fact that the data in algorithm memory 26 was first created by something other than BIST controller 4 before being stored in algorithm memory 26, e.g., at the time of manufacture, does not, in my view, preclude BIST controller 4 from "producing" that data during *operation* of the built-in selft-test circuit. Finally, the fact that BIST controller 4 does not include a compiler is irrelevant, in my view, because BIST controller 4 does not need a compiler in order to "produce" address and control signals; when "invoked," it "produces" them by retrieving them from its memory—i.e., algorithm memory 26—and outputting them.

The *only* scenario in which BIST controller 4 "receives address signals from another component . . . and merely outputs the same address signals," as the majority opinion finds, is in an *alternative* mode of operation described at column 5, lines 41–49, where Averbuj discloses that "user interface 22 may programmably receive algorithms via external input" which are delivered directly to multiplexer 24. That, however, is not the mode of operation relied upon by Petitioner.

For all of the foregoing reasons, I disagree with the majority's finding that "[i]n Averbuj, the algorithms (i.e., CMD_DATA containing OP CODE such as SET ADDRESS) communicated to sequencers 8 are . . . generated by another component (i.e., a component that is not part of BIST controller 4 circuitry) and stored in algorithm memory 20." Maj. Op. 31.

Because I am persuaded that Petitioner has established sufficiently that BIST controller 4 "produces" the recited "address and control signals," I would have analyzed the remainder of Patent Owner's arguments.