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Paper 13
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ADVANCED MICRO DEVICES, INC.,
Patent Owner.

Case IPR2015-00329
Patent 6,266,715 B1

Before BRIAN J. MCNAMARA, RAMA G. ELLURU, and JAMES B. ARPIN, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

LG Electronics, Inc. ("Petitioner") filed a Petition (Paper 2; "Pet.") to institute an *inter partes* review of claims 1, 10, 13, 22, 24, and 25 (the "challenged claims") of Patent No. US 6,266,715 B1 to Loyer *et al.* (Ex. 1001, "the '715 patent"), pursuant to 35 U.S.C. §§ 311–319. Pet. 1. Petitioner indicates that LG Electronics U.S.A., Inc. and LG Electronics MobileComm U.S.A., Inc. are real parties-in-interest. *Id.* Advanced Micro Devices, Inc. ("Patent Owner") filed a Preliminary Response (Paper 12; "Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314,[1] which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Petitioner relies upon the following references and declaration in

[1] *See* Section 6(a) of the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 116 Stat. 284, 300 (2011).

support of its grounds for challenging the identified claims of the '715 patent:

Exhibit	References and Declaration
1003	Declaration of Nader Bagherzadeh, Ph.D.
1004	USBN9602 (Universal Serial Bus) Full Speed Function Controller with DMA Support, National Semiconductor Corporation (www.national.com) (1997) ("USBN9602")
1005	File History of Patent Application No. 08/918,013 (filing date Aug. 25, 1997)
1006	Intel 8237/8237-2 High Performance Programmable DMA Controller, Intel, pp. B-92–105 (Jan. 3, 1984) ("Intel 8237")
1009	USB Function Controller (USBFC), EIFUFAL501 User's Manual (Rev. 2.0), Seiko Epson Corporation (1998) ("EIFUFAL501")
1011	Multi-Endpoint USB Peripheral Controller, Standard Microsystems Corporation (SMSC™) (Rev. 2) (1998) ("USB97C100")
1012	Screenshots of Internet Archive: Wayback Machine (Standard Microsystems' Website) https://archive.org/web/ (Nov. 26, 2014)
1013	Patent No. US 6,185,641 B1 to Dunnihoo (filing date May 1, 1997) ("Dunnihoo")

Petitioner asserts that the challenged claims are unpatentable on the following grounds (Pet. 14–58):

Claims	Grounds	References
1, 10, and 25	35 U.S.C. § 103(a)	USBN9602 (Ex. 1004) and Intel 8237 (Ex. 1006)
1, 10, and 25	35 U.S.C. § 103(a)	EIFUFAL501 (Ex. 1009) and Intel 8237 (Ex. 1006)
1, 10, 13, 22, 24, and 25	35 U.S.C. § 103(a)	USB97C100 (Ex. 1011) and Dunnihoo (Ex. 1013)

For the reasons set forth below, we determine that, on this record, Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing the unpatentability of any of the challenged claims. Accordingly, we *deny* institution of *inter partes* review as to claims 1, 10, 13, 22, 24, and 25 of the '715 patent.

B. Related Proceedings

Petitioner was sued for infringement by Patent Owner: *Advanced Micro Devices, Inc. v. LG Elecs., Inc.*, Case No. 5:14-cv-01012-SI (N.D. Cal.). Pet. 1. Petitioner has filed petitions to review several of Patent Owner's other patents – Patent Nos. US 5,898,849; US 6,889,332 B2; and US 6,895,520 B1.

C. The '715 Patent

The '715 patent is directed generally to "a universal serial bus [("USB")] controller with a direct memory access ('DMA') mode." Ex. 1001, col. 1, ll. 6–8. Each function in the USB device has its own "endpoint," which has its own unique address. *Id.* at col. 2, ll. 51–52. Endpoints are "the ultimate consumer or provider of data." *Id.* at col. 2, ll. 52–56). Specifically, endpoints are used for transmitting and receiving data between the USB host and the functions on the USB device. Ex. 1003 ¶ 36. In addition, all endpoints are one-directional. *Id.* DMA is a capability in computer and peripheral device architectures that allows data to be transferred between two memory locations without using a microprocessor, e.g., the central processing unit ("CPU"). Ex. 1001, col. 1, l. 60–col. 2, l. 16.

The embodiment of Figure 2 of the '715 patent, including our annotations in red, is reproduced below:

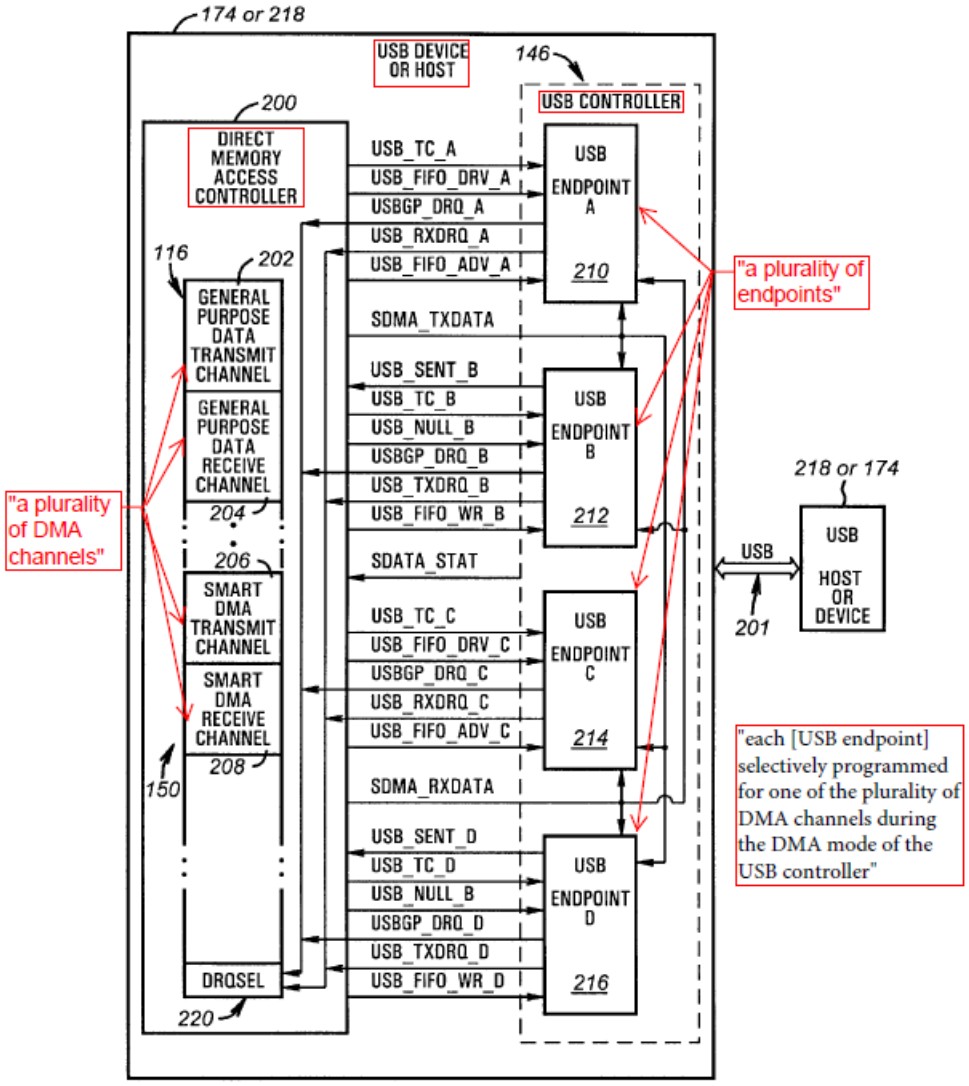


FIG. 2

Figure 2, as annotated, describes USB host 218 or device 174 that includes DMA controller 200 and USB controller 146. Ex. 1001, Fig. 2. An example USB host is a computer system (*id.* at col. 3, ll. 44–45), and an example USB device is a computer peripheral (*id.* at col. 2, l. 46). In Figure 2, DMA controller 200 includes a plurality of DMA channels 202, 204, 206, and 208, and USB controller 146 includes a plurality of USB endpoints 210, 212,

214, and 216. *Id.* at col. 6, l. 56–col. 7, l. 25. Each USB endpoint is programmed selectively for one of the DMA channels. *Id.* at col. 7, ll. 44–48.

D. Illustrative Claim

Petitioner challenges claims 1, 10, 13, 22, 24, and 25 of the '715 patent. Claims 1, 13, and 25 are independent. Claim 10 depends directly from independent claim 1, directed to a USB device; and each of claims 22 and 24 depends directly from claim 13, directed to a USB host. Independent claim 25 is directed to a USB controller.

Claim 1 is illustrative and is reproduced below:

> 1. A universal serial bus (USB) device for USB transfer with direct memory access (DMA), comprising:
>
> a DMA controller, comprising:
>
> a plurality of DMA channels for performing data transfer between the USB device and a USB host; and
>
> a USB controller having a DMA mode, comprising:
>
> a plurality of USB endpoints, *each selectively programmed for one of the plurality of DMA channels during the DMA mode of the USB controller*.

Ex. 1001, col. 11, ll. 59–67 (emphasis added). The disputed limitation is emphasized.

E. Claim Construction

Consistent with the statute and the legislative history of the AIA, we interpret claims of an unexpired patent using the broadest reasonable interpretation in light of the specification of the patent. 37 C.F.R.

§ 42.100(b); *In re Cuozzo Speed Techs. LLC*, No. 2014-1301, slip op. at 16–19 (Fed. Cir. July 8, 2015) ("Congress implicitly approved the broadest reasonable interpretation standard in enacting the AIA," and "the standard was properly adopted by PTO regulation."); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the specification. *See In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An applicant may rebut that presumption by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, limitations are not to be read from the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Petitioner proposes a specific construction for each of the following terms. Pet. 9–11.

1. "DMA mode" (Claims 1, 13, and 25)

Petitioner proposes defining DMA mode as the "mode where a DMA channel is used as part of the process of transferring USB packets between a USB host and a USB device." Pet. 10. Petitioner contends that the term is not defined in the Specification and this definition is not inconsistent with the Specification. *Id.* (citing Ex. 1001, col. 3, ll. 30–45 ("In a DMA mode, a [USB] transmit endpoint of the USB controller *may* be programmed for a [DMA] transmit channel, or a [USB] receive endpoint of the USB controller *may* be programmed for a [DMA] receive channel.")(emphases added). Patent Owner does not disagree. *See* Prelim. Resp. 6–7.

We are persuaded that, on this record and for purposes of this decision, Petitioner's proposed construction is the broadest reasonable interpretation consistent with the ordinary and customary meaning of the term and with the Specification of the '715 patent.

2. "DMA channel" (Claims 1, 13, and 25)

Petitioner contends that the term "DMA channel" should be defined as "a path for moving data directly to or from memory locations without processor intervention." Pet. 11. Petitioner contends that the term is not defined in the Specification and this definition is not inconsistent with the Specification. *Id.* (citing Ex. 1001, col. 2, ll. 18–20 ("The Specification states that '[s]pecific channels are implemented in a DMA unit to allow peripheral devices to transfer data *directly to or from* other peripheral devices or memory devices.'")(emphasis added). Patent Owner does not disagree. *See* Prelim. Resp. 7. We are persuaded that, on this record and for purposes of this decision, Petitioner's proposed construction is the broadest reasonable interpretation consistent with the ordinary and customary meaning of the term and with the Specification of the '715 patent.

As noted above, Patent Owner does not contest these constructions or propose alternatives. *See* Prelim. Resp. 6–7. For purposes of this decision and on this record, no other claim terms require express construction.

II. ANALYSIS

A. Overview

Petitioner argues that claims 1, 10, 13, 22, 24, and 25 of the '715 patent are rendered obvious by the combinations of references described above. *See supra* Section I.A. A patent claim is unpatentable under

35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter[,] as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[2] and (4) objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). On this record and for the reasons set forth below, we are persuaded that Petitioner fails to demonstrate a reasonable likelihood of prevailing in the challenges to claims 1, 10, 13, 22, 24, and 25 of the '715 patent.

B. Asserted Grounds

1. Printed Publications

Petitioner argues that each of the applied references is a printed publication that may be asserted properly as a basis for a ground of unpatentability in its Petition seeking *inter partes* review. Pet. 11–14; *see* 35 U.S.C. § 312(a)(3)(A); 37 C.F.R. § 42.104(b)(2). Patent Owner disagrees and contends that Petitioner fails to demonstrate that USBN9602 (Ex. 1004) and EIFUFAL501 (Ex. 1009) are prior art printed publications. Prelim. Resp. 8–17.

[2] Petitioner's declarant proposes a definition for a person of ordinary skill in the art. Ex. 1003 ¶¶ 18, 19. Patent Owner does not challenge Petitioner's declarant's proposed definition and does not propose an alternative. To the extent necessary and for purposes of this decision, we adopt Petitioner's definition.

The U.S Court of Appeals for the Federal Circuit has held that "public accessibility" is the touchstone in determining whether a reference is a "printed publication." *In re Hall*, 781 F.2d 897, 898–99 (Fed. Cir. 1986); *see, e.g.*, *C&D Zodiac, Inc. v. B/E Aerospace, Inc.*, Case IPR2014-00727, slip op. at 20–22 (PTAB Oct. 29, 2014) (Paper 15) (applied reference shown to be publicly accessible); *L-3 Commc'n. Holdings, Inc. v. Power Survey, LLC*, Case IPR2014-00832, slip op. at 11–12 (PTAB Nov. 14, 2014) (Paper 9) (applied reference not shown to be publicly accessible). "A reference is publicly accessible 'upon a satisfactory showing that such document has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.'" *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008) (quoting *SRI Int'l, Inc. v. Internet Sec. Sys. Inc.*, 511 F.3d 1186, 1194 (Fed. Cir. 2008)) (alteration in original). Whether a reference is a printed publication is a legal question "based on underlying factual determinations." *Id*. (citation omitted). The party seeking to introduce the reference "should produce sufficient proof of its dissemination or that it has otherwise been available and accessible to persons concerned with the art to which the document relates and thus most likely to avail themselves of its contents." *In re Wyer*, 655 F.2d 221, 227 (CCPA 1981) (citation omitted).

a. USBN9602 (Ex. 1004)

USBN9602 is a preliminary technical specification prepared by National Semiconductor Corporation for a Full Speed Function (USB) Controller with DMA Support. Pet. 12 (citing Ex. 1004, 1). Petitioner asserts that USBN9602 "qualifies as prior art at least under 35 U.S.C.

§102(a), because, as indicated by the date on the document, it was published in November 1997, before the June 1, 1998 filing date of . . . the '715 patent." *Id.* (citations omitted). Referring to the first page of USBN9602, we note that the reference bears the following copyright notation: "© 1997 National Semiconductor Corporation" at the bottom of the page and the notation: "PRELIMINARY November 1997" at the top of the page. Ex. 1004, 1. Further, USBN9602 was listed on an Information Disclosure Statement ("IDS") filed on February 12, 1998, in an unrelated patent application, U.S. Patent Application No. 08/918,013. Ex. 1005, 100. Petitioner argues that together the dates on the face of the document and the document's citation in the IDS evidence that USBN9602 was published, i.e., publicly available, prior to the June 1, 1998 filing date of the '715 patent. Pet. 12.

Patent Owner contends, however, that neither the dates on the face of the document nor the document's citation in the IDS evidence that USBN9602 was published, i.e., publicly available, before June 1, 1998. Prelim. Resp. 9. Specifically, Patent Owner contends that Petitioner produces no evidence that National Semiconductor Corporation disseminated datasheets, such as USBN9602, as of the date on the face of the document. *Id.* at 10–11. Moreover, despite the copyright notice, Patent Owner contends that the use of the word "PRELIMINARY" on the face of the document is evidence that USBN9602 was not published. *Id.* at 11 (citation omitted). Further, Patent Owner suggests that, because the companies were involved in a strategic alliance in 1997, 3Com Corporation,

the assignee of the U.S. Patent Application No. 08/918,013,[3] may have obtained an unpublished copy of the USBN9602 from National Semiconductor Corporation. *Id.* at 12–14 (citing Exs. 2005–2008).

When determining the threshold issue of whether a document is a printed publication for purposes of a decision on institution, a copyright notice has been accepted a prima facie evidence of publication.[4] *See Ford Motor Co. v. Cruise Control Techs. LLC*, Case IPR2014-00291, slip op. at 7–8 (PTAB June 29, 2015) (Paper 44) (citing *FLIR Sys., Inc. v. Leak Surveys, Inc.*, Case IPR2014-00411, slip op. at 18–19 (PTAB Sept. 5, 2014) (Paper 9)). Although citation in an IDS *alone* is insufficient to demonstrate that a document is a printed publication, Petitioner does not rely here on the IDS citation alone. *See Microsoft Corp. v. Biscotti Inc.*, Case IPR2014-01457, slip op. at 25–28 (PTAB Mar. 19, 2015) (Paper 9). Although we are not bound by the determinations noted above, at this stage of the proceeding, we are persuaded that the presence of a copyright notice, together with the listing of the reference in an IDS, may be taken as some evidence of public accessibility as of a particular date. Moreover, Patent Owner's evidence of the corporations' alliance does not show, beyond mere speculation, that 3Com Corporation obtained a copy of the USBN9602 from National Semiconductor Corporation prior to its publication. Here, we weigh the evidence presented by both parties to determine whether it is reasonably likely that USBN9602 is a printed publication. Consequently, on this record and for purposes of the decision, we are persuaded that Petitioner has

[3] This patent application issued as Patent No. US 6,000,042 (Ex. 2002).
[4] "[A] notice of copyright . . . *may be placed on publicly distributed copies* from which the work can be visually perceived . . . ." 17 U.S.C. § 401(a) (emphasis added).

provided sufficient evidence to demonstrate a reasonable likelihood that USBN9602 is a printed publication.

b. EIFUFAL501 (Ex. 1009)

EIFUFAL501 is a user's manual for the USB Function Controller developed by Seiko Epson Corporation. Ex. 1009, 1, 4. Petitioner asserts EIFUFAL501 qualifies as prior art under 35 U.S.C. §102(a), because, as indicated by the date on the document, it was published on March 24, 1998, before the June 1, 1998 filing date of the '715 Patent. *See id.* at 1. Petitioner relies *solely* on the date printed on the face of EIFUFAL501 as evidence of its publication before June 1, 1998. Pet. 13.

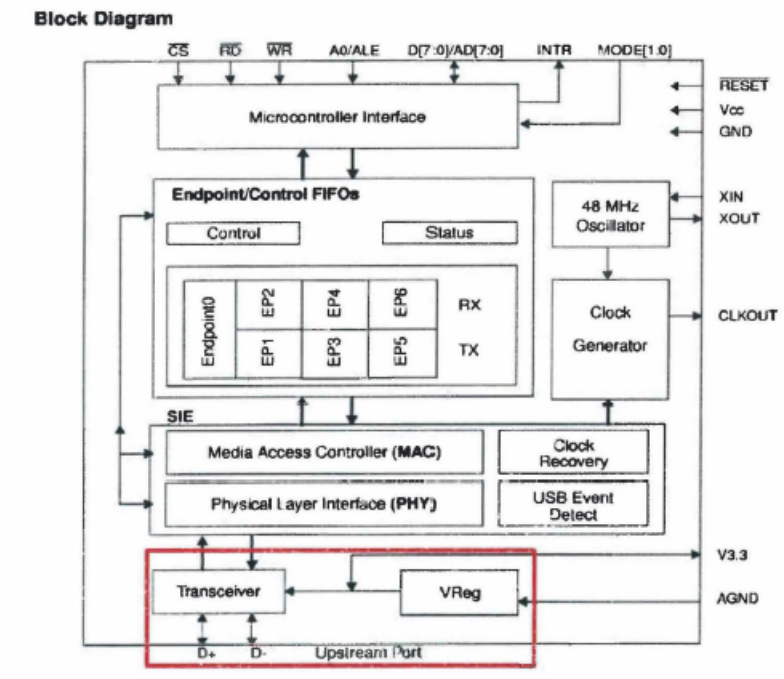
Nevertheless, Petitioner offers no evidence of the nature of this date. *See id.* The date itself only contains the notation "Revision: 2.0," which may suggest that the document was "revised" on March 24, 1998, but is not evidence that it was published on that date. *See* Prelim. Resp. 15. The testimony of Dr. Bagherzadeh, Petitioner's declarant, that EIFUFAL501 was available as of the filing date of the Petition (Ex. 1003 ¶ 49) and his unsupported opinion that EIFUFAL501 "was more than likely published on or about March 24, 1998" (*id.*) is insufficient to demonstrate a reasonable likelihood that EIFUFAL501 was published before June 1, 1998. *See* Prelim. Resp. 15–16. Consequently, on this record and for purposes of this decision, we are not persuaded that Petitioner has demonstrated a reasonable likelihood that EIFUFAL501 is a printed publication.

On this record and for purposes of this decision, we are persuaded that the remaining applied references are printed publications.

2. Obviousness of Claims 1, 10, and 25 over USBN9602 and Intel 8237

As noted above, USBN9602 is a preliminary technical specification

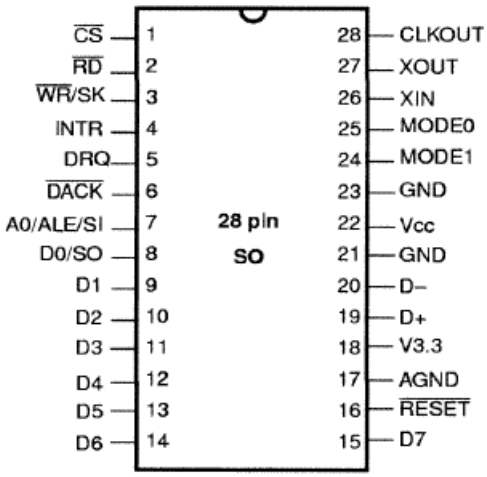
prepared by National Semiconductor Corporation for a USB Full Speed Function Controller with DMA Support. Ex. 1004, 1. A Block Diagram of the USBN9602 controller, including Patent Owner's annotations in red, is reproduced below:



Prelim. Resp. 21; *see* Ex. 1004, 1. This block diagram depicts seven endpoints, Endpoint0 and EP1–EP6, a microcontroller interface, and a transceiver with two pins D+ and D-.

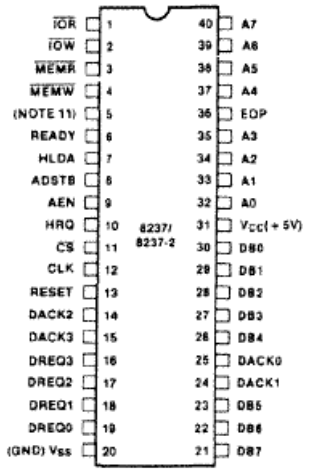
A 4.0 Connection Diagram is reproduced below:

4.0 Connection Diagram



Ex. 1004, 5. This diagram depicts the connections of the USBN9602 controller to other components. In particular, consistent with the Block Diagram of the USBN9602 controller, this diagram depicts pins DRQ and DACK to the DMA controller and pins GND, D+, D-, and V3.3 to and from the USB controller. *Id.* at 1; *see* Prelim. Resp. 22.

Intel 8237 (Ex. 1006) is a technical document prepared by Intel Corporation describing a programmable DMA controller. Ex. 1006, 1. A portion of a Block Diagram depicting the Intel 8237 controller is reproduced below:



Ex. 1006, 1. This diagram depicts the pins of the Intel 8237 controller including four independent DMA channels (Ex. 1006, 1), including pins DREQ0–3 and DACK0–3.

Petitioner contends that the combination of USBN9602 and Intel 8237 DMA teach all of the limitations of claims 1 and 25 and that a person of ordinary skill in the art would have had reason to combine the teachings of these references to achieve the USB device or USB controller, as recited in claims 1 and 25, respectively. Pet. 16, 20–27. In particular, Petitioner argues that a person of ordinary skill in the art would combine the teachings of these references, so that the USB controller could be connected efficiently to memories via a DMA controller. *Id.* at 15. Moreover, the DMA controller of Intel 8237 would allow the various endpoints of the USB controller of USBN9602 to transfer data to memories within a device or host. *Id.* Thus, Petitioner argues that a person of ordinary skill in the art would have had reason to connect the plurality, i.e., seven, of endpoints of the USBN9602 controller with the plurality, i.e., four, of DMA channels of the Intel 8237 DMA controller. *Id.* at 17.

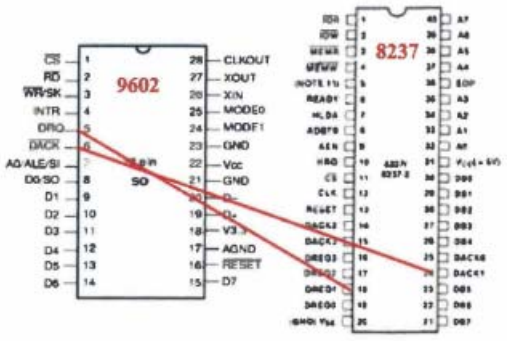
Recognizing that the USBN9602 controller teaches only a limited number of communication pins, which may be connected to the DMA channels of the Intel 8237 controller, Petitioner argues that a person of ordinary skill in the art would have had reason to combine the teachings of two USBN9602 controllers with that of the Intel 8237 controller to achieve the USB device or USB controller, as recited in claims 1 and 25, respectively. *Id.* Specifically, a person of ordinary skill in the art would have had reason to add a second USBN9602 controller because it would increase the number of endpoints available for connection to the DMA controller channels in the USB device or controller. *Id.*

Patent Owner contends that the combination of the teachings of USBN9602 with that of Intel 8237 does not teach or suggest all of the limitations of claims 1 and 25. Prelim. Resp. 23–24. Claims 1 and 25 recite "a plurality of USB endpoints, *each selectively programmed for one of [the/a] plurality of DMA channels during the DMA mode of the USB controller*." Ex. 1001, col. 11, ll. 65–67, col. 13, ll. 40–42 (emphasis added). Petitioner acknowledges that, although this limitation may be construed to provide for each USB endpoint to be programmed for a *different* DMA channel, the claim language does not require that construction. Pet. 18. Instead, Petitioner suggests that limitation may be construed to provide for each USB endpoint to be programmed for the *same* DMA channel. *Id.* (citing Ex. 1003 ¶¶ 66, 67). We disagree.

Dr. Bagherzadeh's testimony concerning this construction is opinion testimony, entirely unsupported by proposed meanings for the individual claim terms defining this limitation, citations to the Specification of the '715 patent, or interpretations given to similar structures or functions in the

relevant art by persons of ordinary skill in the art. Ex. 1003 ¶¶ 66, 67 ("I believe that it is appropriate to disclose *how I read* the plain language of the claim.") (emphasis added). We are not persuaded that Petitioner's construction is the broadest reasonable interpretation of this limitation. *See Translogic Tech. Inc.*, 504 F.3d at 1257. We are persuaded by Patent Owner's contention that each USB endpoint is programmed for a *different* DMA channel. Prelim. Resp. 1. Patent Owner's construction of the limitation is consistent with the Specification of the '715 patent. *Id.* In particular, the Specification of the '715 patent describes that "*[e]ach* USB endpoint is associated with a USB endpoint register (e.g., USB transmit register or USB receive register) or register set 502 or 504 (FIG. 5) for programming the USB endpoint for a *particular* DMA channel." Ex. 1001, col. 7, ll. 44–48 (emphases added); s*ee also* Ex. 1001, col. 2, ll. 17–19 ("Specific channels are implemented in a DMA unit to allow peripheral devices to transfer data directly to or from other peripheral devices or memory devices.").

Noting the pins taught by each reference, Patent Owner contends that the combination of their teachings would link a single endpoint with a DMA channel, as indicated in the annotated figure reproduced below. Prelim. Resp. 24.



This annotated figure shows only a single DMA channel linking pins DRQ and DACK of the USBN9602 controller to pins DREQ1 and DACK1 of the Intel 8237 controller, respectively. *Id.* Patent Owner contends that a person of ordinary skill in the art would not combine the teachings of USBN9602 and Intel 8237 to achieve the USB device or the USB controller recited in claims 1 and 25, respectively, because such a combination only permits one of the plurality of endpoints of USBN9602 to be connected to one DMA channel of Intel 8237 at a time. *Id.* (citing Ex. 1004, 12 ("Only one Endpoint can be enabled at a given time to issue a DMA request when data is received or transmitted.")). Thus, Patent Owner contends that Petitioner fails to demonstrate that the proposed combination of the teachings of USBN9602 and Intel 8237 teaches selectively connecting each endpoint with one DMA channel during the DMA mode. *Id.* We agree with Patent Owner's reasoning.

In addition, Patent Owner contends that a person of ordinary skill in the art would not have had reason to combine the teachings of two USBN9602 controllers and an Intel 8237 controller in the manner proposed by Petitioner. *Id.* at 25–29. We agree with Patent Owner's contention that Petitioner's proposed combination of two USBN9602 controllers would not necessarily teach the same Function Address for each of the plurality of endpoints. Prelim. Resp. 28. USBN9602 teaches that, "[a]ccording to the USB specification, up to 31 such endpoint pipes are supported at any given time, *each with the same Function Address*." Ex. 1004, 4 (emphasis added). Consequently, Petitioner fails to demonstrate that the proposed combination of the teachings of two USBN9602 controllers, each controlling its own distinct USB function (*see* Ex. 2004, 29), with the teachings of Intel 8237

achieves the limitations of the USB device or the USB controller, as recited in claims 1 and 25, respectively. *See* Prelim. Resp. 28.

Moreover, Petitioner argues that a person of ordinary skill in the art would have reason to add the teachings of a second USBN9602 controller "because it would allow the USB device to have more endpoints available." Pet. 17 (citing Ex. 1003 ¶ 63). Additionally, Petitioner argues that adding the second USBN9602 controller only requires connecting, among other signals, the DRQ and DACK pins of the second USBN9602 controller to, for example, the DREQ2 and DACK2 pins of the Intel 8237 controller. *See* Ex. 1004, 5, Fig. 1; Ex. 1006, 1; Ex. 1003 ¶ 63. Patent Owner disagrees. We ae persuaded by Patent Owner's contention that a person of ordinary skill in the art would not have had reason to combine the teachings of two USBN9602 controllers because USBN9602 controllers support USB functions with up to sixteen input endpoints and sixteen output endpoints. Prelim. Resp. 28 (citing Ex. 2004, 47); *see also* Ex. 1004, 4 ("According to the USB specification, up to 31 such endpoint pipes are supported at any given time . . . ."). Further, in view of the insufficient reasons provided by Petitioner for combining two USBN9602 controllers with an Intel 8237 controller, we also are persuaded that Petitioner's proposed reason for combining the teachings of these references is based on hindsight improperly gleaned from the challenged claims. Prelim. Resp. 28 (citing *KSR*, 550 U.S. at 421).

For the reasons set forth above, we are not persuaded that Petitioner has shown that the combined teachings of USBN9602 and Intel 8237 teach or suggest all of the limitations of the USB device or the USB controller, as recited in claims 1 and 25, respectively. Moreover, we are not persuaded

that Petitioner has shown that a person of ordinary skill in the art would have had reason to combine the teachings of these references in the manner that Petitioner proposes. Therefore, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that claims 1 and 25 are rendered obvious by the teachings of *one or more* USBN9602 controllers and the Intel 8237 controller. Because we are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge with respect to the independent claim 1, we also are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge with respect to claim 10, which depends from independent claim 1. Pet. 19–20; *see* Prelim. Resp. 29–31.

3. Obviousness of Claims 1, 10, and 25 under 35 U.S.C. § 103(a) over EIFUFAL501 and Intel 8237

Petitioner asserts that claims 1, 10, and 25 are unpatentable under 35 U.S.C. § 103(a) over EIFUFAL501 and Intel 8237. Pet. 27–41. Because we are not persuaded that Petitioner has demonstrated a reasonable likelihood that EIFUFAL501 is a printed publication (*see supra* Section II.B.1.b.), we are not persuaded that Petitioner has demonstrated a reasonable likelihood of showing that claims 1, 10, and 25 are unpatentable under 35 U.S.C. § 103(a) over EIFUFAL501 and Intel 8237.

4. Obviousness of Claims 1, 10, 13, 22, 24, and 25 under 35 U.S.C. § 103(a) over USB97C100 and Dunnihoo

Petitioner argues that claims 1, 10, 13, 22, 24, and 25 are unpatentable under 35 U.S.C. § 103(a) over USB97C100 and Dunnihoo. Pet. 41–58. USB97C100 (Ex. 1011) is a technical specification prepared by Standard Microsystems Corporation for a USB peripheral controller. Ex. 1011, 1. USB97C100 qualifies as prior art at least under 35 U.S.C. §102(a), because,

as indicated by the copyright date on the document (Ex. 1011, 80 ("1998© STANDARD MICROSYSTEMS CORP.")) and based on the date that it was first available on-line (Ex. 1012, 4), USB97C100 was a printed publication at least by May 23, 1998, and before the June 1, 1998 filing date of the'715 Patent.

The USB97C100 controller may be used with a USB client or a USB host. Pet. 41 (citing Ex. 1011, 13–14). Figure 2 of USB97C100, including our annotations in red, is reproduced below:

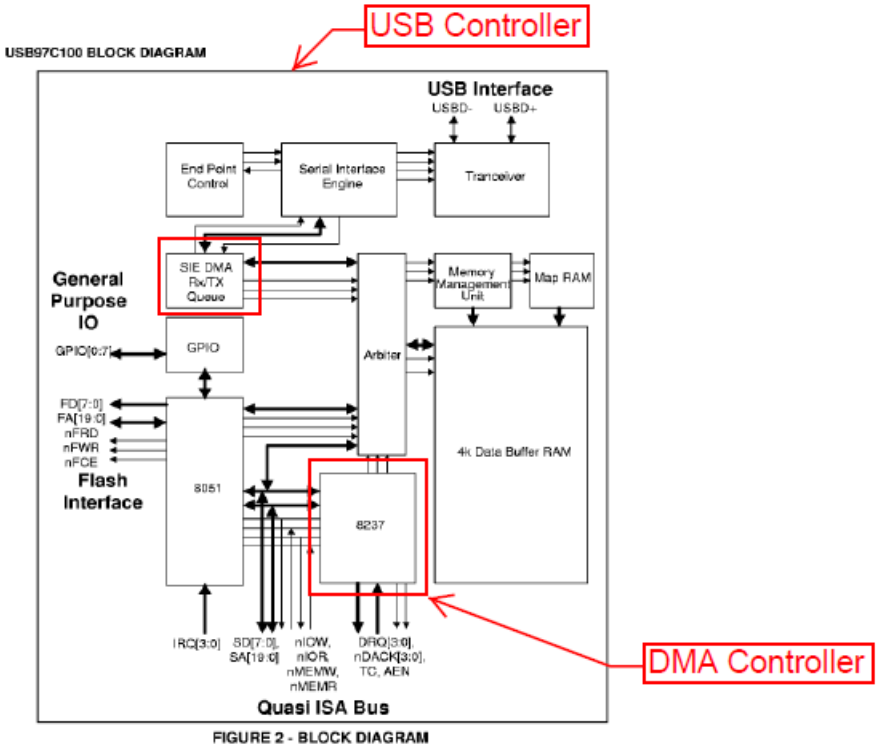


FIGURE 2 - BLOCK DIAGRAM

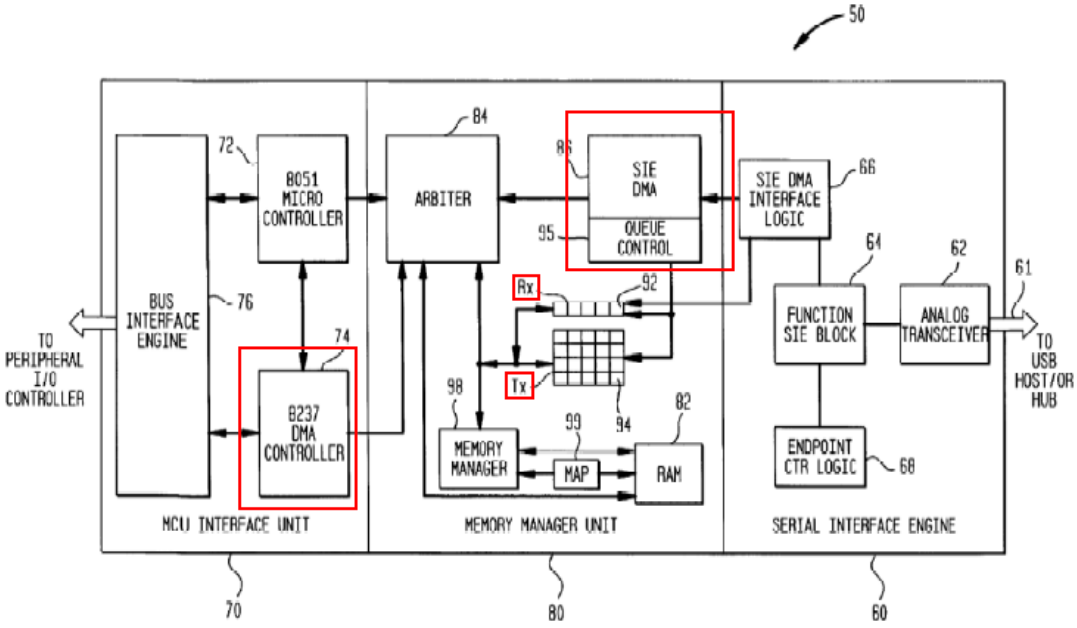
Ex. 1011, 11 (Figure 2). Figure 2 is a Block Diagram of the USB97C100 controller including a Serial Interface Engine ("SIE"), a Serial Interface Engine Direct Memory Access ("SIE DMA"), an Arbiter, a Data Buffer Random-Access Memory ("RAM"), a Memory Management Unit ("MMU"), and an Intel 8237 DMA controller. Pet. 41. Petitioner asserts that

> [t]he SIE is a "USB low-level protocol"' interpreter which controls the USB bus protocol, packet generation/extraction and other functions. [Ex. 1011, 12.] The [Static RAM (SRAM)] supports "16 independent transmit [First In, First Out (FIFO)] queues (one for each endpoint), and a single receive queue" by using a dynamic buffer architecture.

Pet. 42 (citing Ex. 1011, 12, 62; Ex. 1003 ¶¶ 95–97). Thus, USB97C100 teaches the combination of a USB controller, including a plurality of USB endpoints, and a DMA controller.

Dunnihoo (Ex. 1013) discloses a peripheral microcontroller for providing a USB connection to existing peripheral architectures. Ex. 1013, Abstract. Dunnihoo identifies Standard Microsystems Corporation as assignee on its face. Pet. 42. Figure 3 of Dunnihoo, including our annotations in red, is reproduced below:

FIG. 3



Ex. 1013, Fig. 3. Figure 3 of Dunnihoo depicts a USB controller including SIE 60, Microcontroller Interface Unit ("MCU Interface Unit") 70, including Intel 8237 DMA controller 74, and Memory Management Unit ("MMU")

80. Pet. 42–43. Petitioner argues that Dunnihoo discloses a DMA controller with a DMA channel because Dunnihoo's DMA controller discloses that the "memory management unit includes a first DMA controller for providing *a data path* between said first Interface and said RAM." *Id.* at 46 (quoting Ex. 1013, Claim 3 (emphasis added)). Petitioner argues that Dunnihoo's "data path is equivalent to a DMA channel because DMA channels are designed to provide a path for data between two memory locations." *Id.* (citing Ex. 1003 ¶ 108). In particular, Petitioner argues that Dunnihoo teaches transferring data between SIE 60 and RAM 82. *Id.*

Petitioner further argues that a person of ordinary skill in the art would have combined the teachings of USB97C100 and Dunnihoo for several reasons. *Id.* at 43–44. Petitioner argues that USB97C100 and Dunnihoo disclose similar devices having similar components. *Id.* Specifically, Petitioner argues that a person of ordinary skill in the art would have believed that USB97C100 is a commercial embodiment of the device disclosed in Dunnihoo. *Id.* at 44. In addition, Petitioner argues that USB97C100 discloses that the USB97C100 controller "will allow virtually any PC peripheral to be placed at the end of a USB connection." *Id.* (citing Ex. 1011, 5).

Patent Owner contends that Petitioner's construction of a "DMA channel" is inconsistent with Petitioner's application of that construction to Dunnihoo's "data path." Prelim. Resp. 39–42. As noted above, Petitioner construes "data channel" as "a path for moving data *directly to or from memory locations without processor intervention*." *See supra* Section I.E.2. (emphasis added). Petitioner argues that Dunnihoo's DMA controller "discloses that the 'memory management unit includes a first DMA

controller for providing a data path *between said first Interface and said RAM*.'" Pet. 46 (quoting Ex.1013, Claim 3 (emphasis added)). Patent Owner contends that Petitioner does not demonstrate that Dunnihoo's data path moves data *directly to or from memory locations* without processor intervention. Prelim. Resp. 40. Patent Owner also contends that Dunnihoo's data path also moves data to or from memory locations *with* processor intervention. *Id.* at 40–41 (citing Ex. 1013, col. 8, ll. 32–35). We are persuaded that Dunnihoo's data path does not move data *directly* to or from memory locations and that data is moved *with* processor intervention. Consequently, we are not persuaded that Petitioner has demonstrated that Dunnihoo teaches or suggest DMA channels, as recited in the challenged claims.

Petitioner further argues that

> To the extent Dunnihoo fails to disclose a DMA controller comprising a plurality of DMA channels for performing data transfer between the USB device and a USB host, one of ordinary skill in the art would increase the data path to two data paths thereby creating one receive data path ("Receive DMA Channel") and one transmit data path ("Transmit DMA Channel"). [Ex. 1003 ¶ 109.] One of ordinary skill in the art would be motivated to do so because packets from the USB host destined for the Dunnihoo controller's RAM in the USB device and packets from the USB device destined for the USB host would no longer share the same data path, thus increasing the efficiency of the SIE and the Dunnihoo controller as a whole. [*Id.*]

Pet. 46.

Nevertheless, USB97C100 teaches one transmit FIFO DMA queue for *each* endpoint and one receive queue for *all* endpoints. Pet. 42; Ex. 1011, 12. We are persuaded by Patent Owner's contention that

> even if *one* polled "endpoint is selectively programmed for the Transmit DMA channel," as the Petition alleges, Pet. 49, the challenged claims require *each* of the plurality of USB endpoints to be selectively programmed for one of the plurality of DMA channels. The Petition does not explain how *each* of Dunnihoo's alleged endpoints are selectively programmed for one of the plurality of DMA channels.

Prelim Resp. 47. Moreover, we agree with Patent Owner that Petitioner's reason for increasing Dunnihoo's data path to two data paths thereby creating one receive data path and one transmit data path" is insufficiently supported by evidence, and we also are persuaded that Petitioner's proposed reason for combining the teachings of these references is based on hindsight improperly gleaned from the challenged claims. Prelim. Resp. 43; *see id.* at 45–46; *KSR*, 550 U.S. at 421.

For the reasons set forth above, we are not persuaded that Petitioner has shown that the combined teachings of USB97C100 and Dunnihoo teach or suggest all of the limitations of the USB device, the USB host, or the USB controller, as recited in claims 1, 13, and 25, respectively. Moreover, we are not persuaded that Petitioner has shown that a person of ordinary skill in the art would have had reason to combine the teachings of these references in the manner that Petitioner proposes. Therefore, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that claims 1, 13, and 25 are rendered obvious by the teachings of one or more USB97C100 and Dunnihoo. Because we are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge with respect to the independent claims 1 and 13, we also are not persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge with respect to claim 10, which depends from

independent claim 1, or claims 22 and 24, which depend from independent claim 13. *See* Pet. 48–52; Prelim. Resp. 37–48.

III. CONCLUSION

Petitioner fails to demonstrate that there is a reasonable likelihood of prevailing in its challenge to the patentability of claims 1, 10, 13, 22, 24, and 25of the '715 patent. Consequently, the Petition is *denied* as to each of the asserted grounds.

IV. ORDER

For the reasons given, it is

ORDERED that the Petition is *denied*, and no *inter partes* review is instituted.

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