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Paper 13
Entered: June 17, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ADVANCED MICRO DEVICES, INC.,
Patent Owner.

Case IPR2015-00323
Patent 6,889,332 B1

Before JONI Y. CHANG, RAMA G. ELLURU, and JAMES B. ARPIN,
Administrative Patent Judges

ELLURU, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. BACKGROUND

Petitioner, LG Electronics, Inc. ("LG"), filed a Petition requesting *inter partes* review of claims 9, 10, and 13–17 of U.S. Patent No. 6,889,332 B1 ("the '332 patent;" Ex. 1001). Paper 2 ("Pet."). Patent Owner, Advanced Micro Devices, Inc. ("AMD"), filed a Preliminary Patent Owner Response. Paper 12 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. §§ 6(b) and 314.

Under 35 U.S.C. § 314(a), an *inter partes* review may be instituted only if "the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." *See* 37 C.F.R. § 42.108(c).

For the reasons given below, on this record we find that LG has not established a reasonable likelihood of prevailing with respect to at least one challenged claim of the '332 patent. Accordingly, we deny the Petition and decline to institute an *inter partes* review of the '332 patent.

A. Related Proceedings

The parties represent that the '332 patent is the subject of the following district court action: *Advanced Micro Devices, Inc., et al. v. LG Electronics, Inc. et al.*, Case No.3:14-cv-01012-SI (N.D. Cal.). Pet. 1; Paper 3, 2. LG also has filed additional petitions challenging different patents. Pet. 1–2.

B. The '332 Patent

The '332 patent is directed to power management of computer systems. Ex.1001, 1:8–9. In particular, the invention is directed to changing the maximum available performance state of a processor in a computer system according to temperature so that a more gradual reduction in performance is provided as temperature increases. *Id*. at Abstract. This gradual reduction in performance results in higher average system performance as temperature

increases. *Id*. The '332 patent Specification explains that "a more gradual reduction in performance is provided while still maintaining a high speed rating of the processor in more ideal conditions." *Id*. Figure 4 from the '332 patent is reproduced below.

Temperature	Type of Trip Point	Action	Available Performance States	Temp Range
103C	Critical Trip Point	OS performs orderly shut down	P2, P3, P4	>80C
98C	Passive Trip Point (max active cooling)	OS throttles processor (50%)		
≥80C	Maximum Pstate Change	Transition to Pstate2 as max		
≤78C	Maximum Pstate Change	Transition to Pstate1 as max	P1, P2, P3, P4	70-80C
≥70C	Maximum Pstate Change	Transition to Pstate1 as max		
≤68C	Maximum Pstate Change	Transition to Pstate 0 as max	P0, P1, P2, P3, P4	<70C
65C	Active trip point 2 (max active cooling)	Turn on Fan 100%		
60C	Active trip point 3 (med active cooling)	Turn on Fan 66%		
50C	Active trip point 4 (min active cooling)	Turn on Fan 33%		

Figure 4 "illustrates an exemplary set of temperature 'trip points' at which power management activities take place." *Id*. at 6:57–59. In this embodiment, both the number of performance states and the maximum performance state changes based on temperature trip points of 70º C and 80º C. *Id*. at 7:30–33. The '332 Specification describes the embodiment illustrated in Figure 4 as follows:

> [W]hen the die temperature is below 70 C, all the performance states are available (PO–P4) and the maximum performance state available, e.g., for utilization based (or other) power management activities, is the maximum performance state that the system provides, namely PO. When the temperature is between 70 C and 80 C, the performance states available are Pl–P4 with the maximum available performance state being Pl. Finally, when the temperature crosses above 80 C the

> available performance states are further reduced, with the maximum available performance state being P2 . . . . When the temperature falls back into a temperature range, e.g., <70 C, the higher maximum performance state once again becomes available.

Id. at 7:19–36. The '332 patent Specification further explains that performance states are "typically based on such factors as operating frequency and voltage." *Id*. at 2:15–16.

C. Illustrative Claim

LG challenges claims 9, 10, and 13–17 of the '332 patent. Claims 9, 15, and 17 are independent. Claims 10, 13, and 14 depend directly or indirectly from claim 9, and claim 16 depends from claim 15. Claim 9 is illustrative of the claimed subject matter and recites:

> 9. A computing system comprising:
>
> an integrated circuit operable at multiple performance states, the performance states being defined by at least one of operating voltage and frequency;
>
> and wherein the computing system provides that the integrated circuit, at a first detected temperature, has a first maximum performance state and a first plurality of lesser performance states; and wherein at a second detected temperature, higher than the first detected temperature, the integrated circuit has a lower maximum performance state and a second plurality of lesser performance states, the lower maximum performance state providing lower performance than the first maximum performance state in terms of maximum power consumption; and wherein the lower maximum performance state is one of the first plurality of lesser performance states.

D. References Relied Upon

LG relies upon the following references (Pet. 10–11):

> U.S. Patent No. 6,311,287 B1, pursuant to 35 U.S.C. §§ 102(a) and 102(e), filed October 11, 1994, and issued October 30, 2001 (Ex. 1003) ("Dischler")

U.S. Patent No. 6,470,290 B1, pursuant to 35 U.S.C. § 102(e), filed August 31, 2000 (Ex. 1004) ("Lee")

U.S. Patent No. 6,535,798 B1, pursuant to 35 U.S.C. § 102(e), filed December 3, 1998 (Ex. 1006) ("Bhatia")

LG also provides the declaration of Paul Min, Ph.D. in support of its petition. Ex. 1002.

E. The Asserted Challenges

LG argues that challenged claims 9, 10, and 13–17 are unpatentable based on the following grounds (Pet. 11):

References	**Basis**	**Claim(s)**
Dischler	§§ 102(a) and (e)	9, 10, 13–17
Lee	§ 102(e)	9, 10, 13–16
Lee	§ 103(a)	13, 17
Bhatia	§ 102(e)	9, 10, 13–16[1]
Bhatia	§ 103(a)	17

II. ANALYSIS

A. Claim Interpretation

In determining whether to institute a review, we construe the claims. In an *inter partes* review, a claim in an unexpired patent is given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1278–82 (Fed. Cir. 2015) ("Congress implicitly adopted the broadest reasonable interpretation standard in enacting the AIA," and "the standard was properly

[1] While LG's table of asserted grounds with respect to Bhatia (Pet. 11) asserts that Bhatia anticipates claim 17, LG's analysis of Bhatia argues that Bhatia anticipates claims 9, 10, and 13–16 (Pet. 43–56). Thus, we do not consider whether Bhatia anticipates claim 17.

adopted by PTO regulation."). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). We determine that, for purposes of our decision, we need not provide an express construction for any of the claim terms.

B. Dischler (Ex. 1003)

LG contends that claims 9, 10, and 13–17 are anticipated by Dischler. Pet. 11–26.

Dischler discloses a computer system and heat-management algorithms implemented in a microcontroller that respond to a control signal for selecting a maximum clock signal frequency value, in accordance with the operating conditions, including temperature and power consumption. Ex. 1003, Abstract; *see also* Ex. 1003, 2:26–33, 6:31–36. The updated maximum frequency can be higher than, lower than, or the same as the current maximum frequency. *Id.* Dischler describes two different embodiments of the heat management algorithm, one based on predicted temperature and another based on the current temperature read from the thermistor. *Id*. at 7:16–26 (Figure 5B), 7:60–8:4 (Figure 7).

Independent claim 9 recites "multiple performance states" and further "at a first detected temperature" "*a first maximum performance state* and a *first plurality of* lesser *performance states*" and "at a second detected temperature, higher than the first detected temperature . . . *a lower maximum performance state* and *second plurality of lesser performance states*." Similarly, claim 15 recites "*a plurality of* groups of *performance operating states*," each group "having a *different maximum operating state*," and the groups "corresponding to respective different temperature ranges related to operation of a processor." Claim 17 recites "the processor having

a plurality of groups of performance states associated with each of a plurality of temperature ranges." Thus, each of independent claims 9, 15, and 17 recites a plurality of performance (operating) states for each detected temperature (claim 9) or temperature ranges (claims 15 and 17).

In arguing that Dischler discloses "multiple groups of performances states, each group having a maximum performance state and a plurality of lesser performance states," LG refers to Figure 7 of Dischler. Pet. 13 (citing Ex. 1002, ¶ 113). Figure 7 of Dischler is reproduced below.

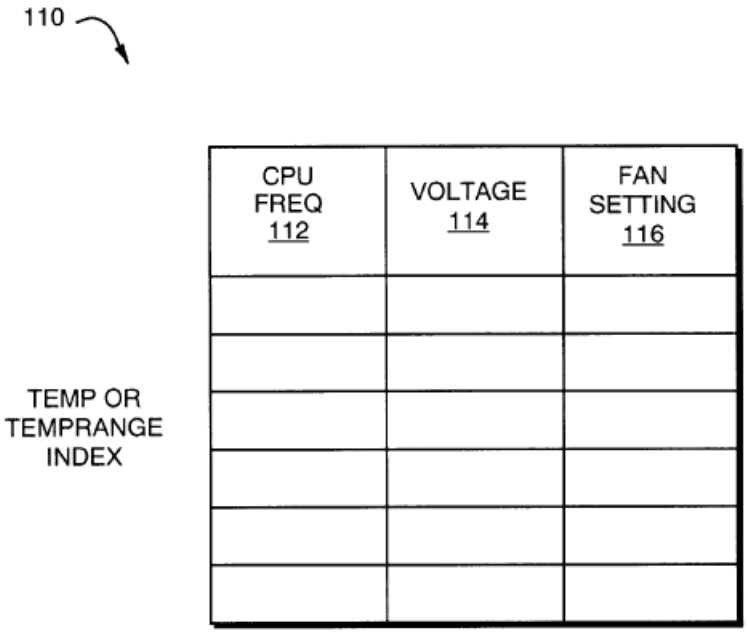

Figure 7 illustrates an algorithm, which can be implemented for heat management, listing available, allowable CPU operating frequencies, acceptable supply voltages corresponding to the operating frequencies, and a fan setting. Ex. 1003, 7:60–67. LG asserts the following about Figure 7.

> Rows for as many as six performance states defined by a frequency and supply voltage are depicted in the table. As such, the table depicted in Fig. 7 illustrates multiple groups of performance states, each group having a maximum performance state and a plurality of lesser performance states.

Pet. 13 (citing Ex. 1002, ¶ 113);[2] *see also* Pet. 15–18 (claim chart for claim 9). According to LG, "[i]f each performance state is labeled from P0 (highest frequency) to P5 (lowest frequency), the groups would include the following:"

Table 1

Group	Available Group of Performance States	Maximum Performance State	Lesser Performance States
1	P0, P1, P2, P3, P4, P5	P0	P1, P2, P3, P4, P5
2	P1, P2, P3, P4, P5	P1	P2, P3, P4, P5
3	P2, P3, P4, P5	P2	P3, P4, P5
4	P3, P4, P5	P3	P4, P5

Pet 13–14 (citing Ex. 1002, ¶ 113). LG has not persuaded us sufficiently that Dischler discloses the recited performance (operating) states of independent claims 9, 15, and 17.

As AMD argues, LG "does not map the alleged performance states to temperature or temperature ranges, as required by the claims." Prelim. Resp. 31–32. In describing Figure 7, Dischler explains that "[t]he current t*emperature* read from the thermistor is used as an index into the table 100 to provide as outputs thereof the next operating *frequency* of the CPU, supply *voltage* of the CPU, and a fan setting of the computer." Ex. 1003, 7:67–8:4 (emphasis added). Thus, based on this record, Dischler associates a single temperature with a single CPU frequency, a single voltage, and a single fan setting, but does not disclose a *plurality* of performance operating states for each current temperature or temperature range, as required by claims 9, 15, and 17. *See* Prelim. Resp. 31–32. LG has not shown adequately how this disclosure anticipates the challenged claims.

Moreover, LG's argument that Dischler anticipates each of the challenged claims is deficient because it improperly relies on two different embodiments from

[2] We agree with AMD that citation to LG's expert declaration is unhelpful because the declaration merely mimics exactly that found in the petition. Prelim. Resp. 32–33.

Dischler. "A reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.'" *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (citation omitted). To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008). A prior art reference "include[ing] multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention," is insufficient to show prior invention. *Id*. at 1371(citation omitted). In *Net MoneyIN*, although a prior art reference described two protocols, which when taken together, disclose "all five links arranged or combined in the same way as claimed," the Federal Circuit determined that the reference did not anticipate the claim. *Net MoneyIN*, 545 F.3d at 1371 ("The district court was also wrong to combine parts of the separate protocols shown in the iKP reference in concluding that claim 23 was anticipated."). Rather, the Federal Circuit stated that, in order to find anticipation, all five links would have to be described in one single example/protocol. *See Id*.

In its challenge to independent claims 9, 15, and 17, LG refers to both Figures 5 and 7 of Dischler. *See* Pet. 15–18, 22, and 25. Figures 5 and 7 disclose two distinctly different embodiments. Figure 5 describes an algorithm for implementing heat management of a computer system wherein a *predicted* temperature is used to determine whether to make changes in operating parameters. Ex. 1003, 6:45–48. And Figure 7 describes an alternative algorithm for implementing heat management of a computer system wherein the *current* temperature is used to calculate an operating frequency and voltage of the processor. *Id*. at 750:–8:4. LG provides no explanation as to how elements from

these two distinctly different embodiments can be combined to disclose prior invention of the challenged independent claims.

Accordingly, we determine that LG has not established a reasonable likelihood of prevailing in showing that independent claims 9, 15, and 17, and, for the same reasons, dependent claims 10, 13, 14, and 16 are anticipated by Dischler.

C. Lee (Ex. 1004)

Lee discloses power management modes which include: "(1) a maximum power performance mode ["MPM"], (2) a battery-optimized mode ["BOM"], and (3) a performance/optimization cycling mode ["POCM"] for performing the maximum performance and the battery-optimized mode alternatively within a prescribed period of time." Ex.1004, Abstract. "[T]he maximum performance mode means a state where the load of the system is maximum and other devices are operated according to this. The battery-optimized mode means idle state of parts of a device, that is, power save state." *Id*. at 1:49–52. Lee further describes the POCM mode as alternately utilizing the

> maximum performance mode (PM) and the battery optimized mode (BOM) for a prescribed period of time D_T based on MPM and BOM duration ratio $R_{P/O}$, where $R_{P/0}=T_P/T_O$, T_P being the cumulative duration of the maximum performance mode for a first prescribed period of time D_1 and T_0 being the cumulative duration of the battery optimized mode for a second prescribed period of time D_2.

Id. at 4:25–35.

> For example, in the preferred embodiment, there are four additional power management modes based on the duration ratio $R_{P/O}$ of POCM1, POCM2, POCM3 and POCM4 for a prescribed period of time D_T of 100 ms. In POCM1, the $R_{P/O}$=4:1, where T_P=80 ms and T_O=20 ms, such that the MPM is performed for 80 ms and thereafter BOM is performed for 20 ms within the 100 ms prescribed period of time D_T.

Id. at 4:36–43.

Anticipation

LG contends that claims 9, 10, and 13–16 are anticipated by Lee. Pet. 27–37. LG has not persuaded us sufficiently that Lee discloses the recited performance (operating) states of independent claims 9 and 15.

Instead, we agree with AMD that claim 9 requires more than two performance states. Prelim. Resp. 37. Claim 9 requires "at a first detected temperature" "a first maximum performance state and a first plurality of lesser *performance states*." Thus, claim 9 recites at a first detected temperature, a maximum performance state and lesser performance "states," in plural form. We further agree with AMD that claim 15 recites more than two performance states. Prelim. Resp. at 37, n.2. Specifically, claim 15 recites "*a plurality of* groups of *performance operating states*," each group "having a *different maximum operating state*," and the groups "corresponding to respective different temperature ranges related to operation of a processor." For example, Group 1 can include a first maximum operating state and a second maximum operating state (the maximum operating state from Group 2). *Id*. Group 2 can include the second maximum operating voltage and another operating state. Because claim 15 recites "groups of performance operating states" ("states" is in plural form), Group 2 must include at least two operating states. *Id*.

LG argues that Lee discloses MPM, BOM, and "the use of intermediate performance states, wherein the processor is cycled between MPM and BOM" and that "[t]hese intermediate performance states are called performance/optimization cycling modes ('POCMs')." Pet. 27–28. LG further refers to Lee's MPM, BOM, and POCMs as disclosing the required "several different performances states" of claims 9 and 15. *Id*. LG, however, has not persuaded us satisfactorily that Lee

discloses more than two performance operating states, as required by claims 9 and 15. As AMD argues (Prelim. Resp. 40), Lee describes the POCM as operating in either the MPM or BOM performance state at any point in time.[3] *See* Ex. 1004, 4:25–64; Prelim. Resp. 36, 40–41. Thus, even assuming that MPM and BOM are distinct performance states (e.g., each with its own operating voltage and/or frequency), each POCM has the same voltage and frequency as either the MPM or the BOM, at any point in time. For this reason, LG has not persuaded us that Lee discloses more than two performance states or performance operating states, as required by claims 9 and 15, respectively.

In addition, LG has not persuaded us that Lee discloses the limitations of claim 9 for the following reason. Claim 9 requires "multiple performance states" "defined by at least one of operating voltage and frequency." As discussed above, LG refers to Lee's MPM, BOM, and POCMs as disclosing a plurality of performance states. Pet. 27–28. Lee describes the MPM as "a state where the load of the system is maximum and other devices are operated according to this." Ex. 1004, 1:49–51. Lee further describes the BOM as an "*idle state* of parts of a device, that is, power save state." *Id*. at 1:51–52 (emphasis added). Lee does not describe either MPM or BOM in terms of either operating frequency or voltage.

LG refers to a Popular Science article in arguing that Lee's MPM is "characterized by a higher clock frequency and voltage than the battery optimizing mode." Pet. 27. The Popular Science article states that,

[3] As AMD explains, a determination that Lee's POCM consists of either a MPM or BOM state at any point in time is consistent with the plain and ordinary meaning of "state," which is "[a] condition that characterizes the behavior of a function/subfunction or element at a point in time." Ex. 2001, 1040 (IEEE Dictionary)

"[p]lugged in, mobile Pentium III notebooks will run at full speed, or 600MHz, but will switch to a lower-voltage 500MHz when *running* on battery power." Ex. 1005, 4 (emphasis added). LG's argument in support of anticipation is deficient because LG relies on more than a single reference. *Net MoneyIN*, 545 F.3d at 1369 (to establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference). Even if consideration of the Popular Science article was proper, LG's argument remains deficient. LG does not provide any analysis as to how the Popular Science article's description of the frequency of the "running" on battery power condition of the Pentium II notebook discloses the frequency of Lee's BOM, which Lee describes as being in the "idle state." *See* Prelim. Resp. 38–39. Thus, LG has not persuaded us sufficiently that Lee discloses "performance states . . . defined by at least one of operating voltage and frequency."

Accordingly, we determine that LG has not established a reasonable likelihood of prevailing in showing that independent claims 9 and 15, and, for the same reasons, dependent claims 10, 14, and 16 are anticipated by Lee.

Obviousness

LG contends that claims 13 and 17 would have been obvious over Lee. Pet. 38–43. Claim 13 depends from claim 10, which depends from claim 9. Except for the additional limitation of claim 13, LG's analysis of claim 13 as having been obvious over Lee relies on its anticipation claim chart for claim 10 (Pet. 41), and LG's anticipation analysis of claim 10 refers to its anticipation claim chart for claim 9 (*id*. 34). For the same reasons discussed above as to why LG has not persuaded us sufficiently that Lee

anticipates claim 9, LG has not persuaded us that claim 13 is obvious over Lee.

LG's analysis of claim 17 as having been obvious over Lee, and specifically the limitation reciting "the processor having a *plurality of groups of performance states* associated with each of *a plurality of temperature ranges*," refers to its anticipation of claim 9. Pet. 42. For the same reasons discussed above as to why LG has not persuaded us sufficiently that Lee anticipates claim 9, LG has not persuaded us that claim 17 is obvious over Lee.

Accordingly, we determine that LG has not established a reasonable likelihood of prevailing in showing that claims 13 and 17 are obvious over Lee.

D. Bhatia (Ex. 1006)

Bhatia discloses "[a] system including a component (e.g., a processor) with a clock and a thermal management controller that monitors a temperature in the system. The thermal management controller varies the component between different performance states (e.g., cycles the processor between a high and a low performance state) *when an over-temperature condition is detected*." Ex. 1006, Abstract (emphasis added), 2:23–27. Bhatia discloses one embodiment in which one low performance state is defined along with a high performance state, and, optionally, one or more intermediate performance states. *Id*. at 2:35–37. For example, "[i]n the HP state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in the LP state, the processor's core clock frequency and voltage level may be at a lower setting." *Id*. at 2:45–48.

In Bhatia's system, "[o]ne or more temperature sensor units 15 monitor system temperature in one or more corresponding thermal zones, each capable of issuing an interrupt, e.g., . . . [a] notification when a sensed temperature rises above a preset target temperature T_t or falls below the target temperature T_t." *Id.* at 3:32–38. Figure 12 of Bhatia is reproduced below.

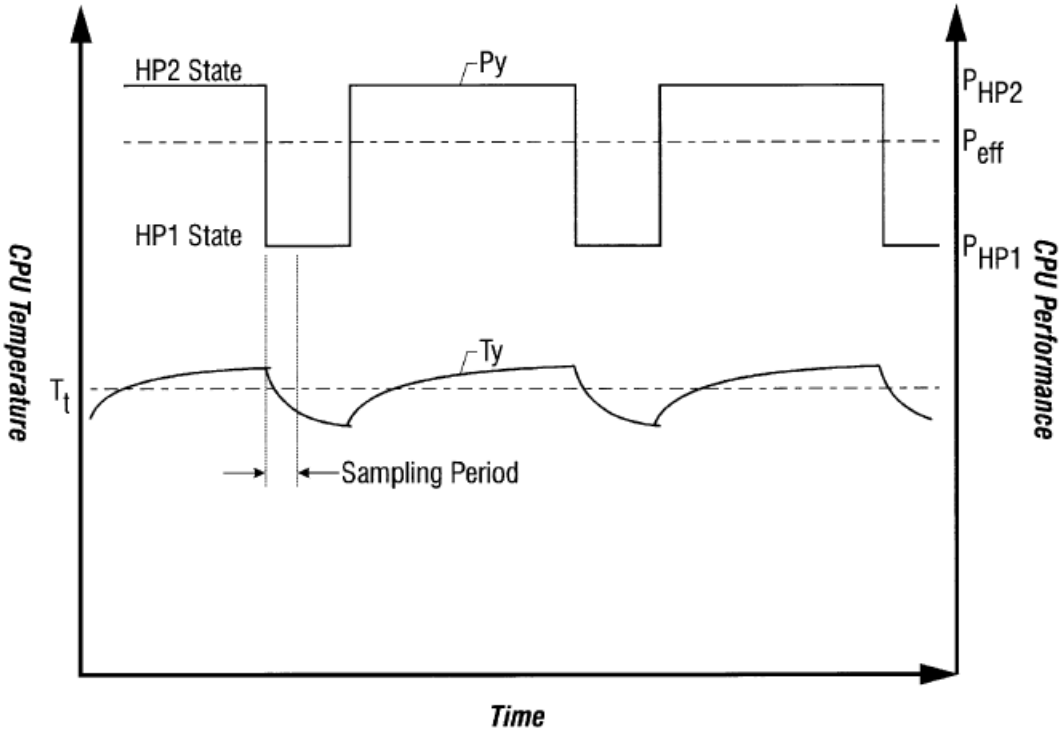

FIG. 12

Figure 12 illustrates a "graph[] of power dissipation levels and temperatures in the system of FIG. 1 when performing thermal management according to further embodiments." *Id.* at 2:14–16. This embodiment defines a lower performance (LP) state and two higher performance states, referred to as the HP1 and HP2 states, wherein the HP2 state has a higher performance level than the HP1 state. *Id.* at 9:46–50. In describing Figure 12, Bhatia states:

> [A] graph is illustrated of the cycling of the power dissipation $\mathbf{P}_y$ between the **HP2** and **HP1** levels. The effective dissipation $\mathbf{P}_{eff}$

> provided by this thermal management scheme lies between P_{HP2} and P_{HP1}, the **HP2** and **HP1** power dissipation levels, respectively. *The temperature graph T_y illustrates the transition of system temperature above and below the target temperature T_t with performance state cycling, with the temperature T_y dropping in the **HP1** state and rising in the **HP2** state*.

Id. at 9:51–59 (emphasis added). In response to an over-temperature condition, the performance state of the processor may be dropped to the HP1 state. *Id*. at 9:63–67. If the decline of the temperature does not occur at a satisfactory rate, the processor may be throttled in the HP1 state. *Id*. at 9:67–10:4.

Figure 14 of Bhatia is reproduced below.

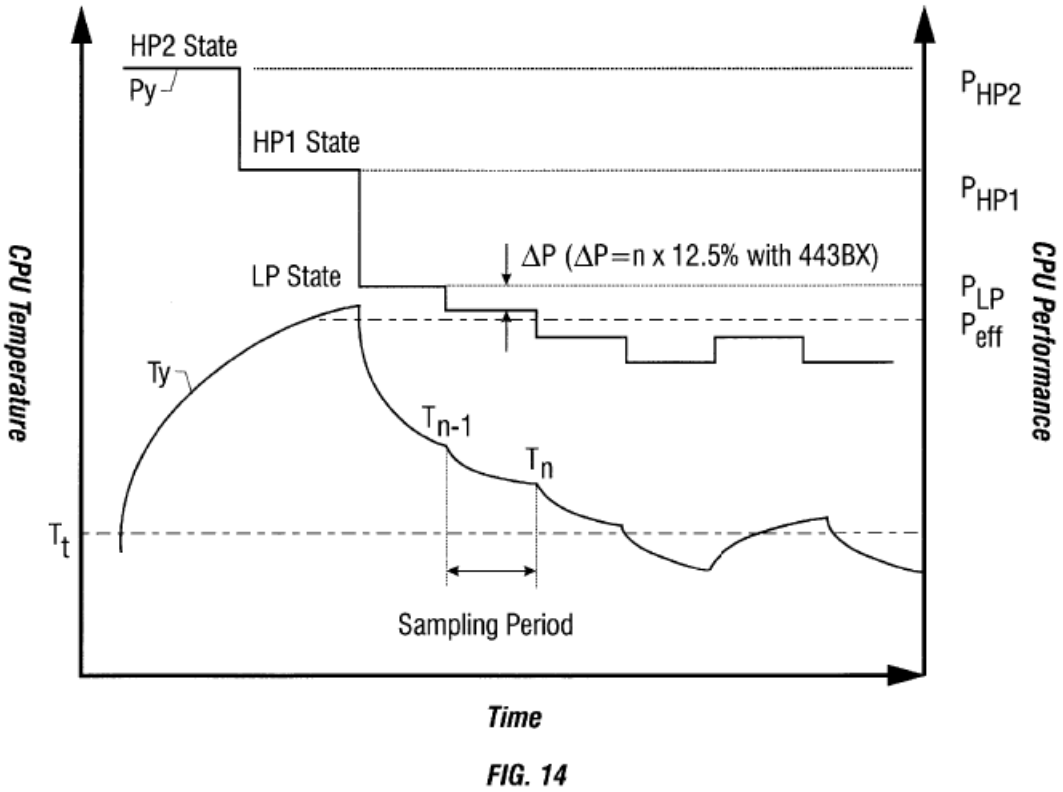

FIG. 14

Figure 14 above shows a "graph[ ] comparing performance levels of the system of different thermal management schemes." *Id.* at 2:17–19. In describing Figure 12, Bhatia states:

> [I]f a temperature $\mathbf{T}_y$ rises above the temperature $\mathbf{T}_t$, the processor **12** is first dropped from the **HP2** state to the **HP1** state. If the temperature does not drop below the target temperature T_t, the processor **12** may further be dropped to the LP state. If further performance level drops are needed to reduce temperature, the processor 12 may then be throttled from the LP state.

Id. at 10:8–18.

Anticipation

LG contends that claims 9, 10, and 13–16 are anticipated by Bhatia. Pet. 43–56. According to LG, "Bhatia teaches the use of three distinct performance groups of performance states depending on temperature: The HP2 and HP1 performance states, states between HP1 and LP, and states at LP and below." Pet. 45 (citing Ex. 1002, ¶¶134, 195).[4] LG further contends that Figure 14 depicts three performance states resulting from throttling the processor in LP mode. Pet. 44–45 (citing Ex. 1006 at Fig. 4; Ex. 1002 at ¶¶130-133). LG concludes, "Bhatia discloses [a] plurality of groups of performance states, wherein each group has a maximum performance state and a plurality of lesser performance states, to manage a computer system's power." Pet. 45. In support, LG provides the following table. *Id.*

[4] As AMD contends (Prelim. Resp. 52), these cited portions of the declaration do not discuss the two "detected temperature(s)" of claim 9 or the "temperature ranges" of claim 15.

Table 5 Bhatia Performance States			
Group	Available Group of Performance States	Maximum Performance State	Lesser Performance States
1 (High Power Mode)	HP2, HP1	HP2	HP1
2 (HP1 Mode)	HP1, performance states between HP1 and LP, LP	HP1	LP, performance states between HP1 and LP
3 (LP Mode)	LP, performance states below LP	LP	Performance states below LP

As discussed above, claim 9 requires two "detected temperature[s]," at each detected temperature "a maximum performance state" and a "plurality of lesser performance states." Similarly, claim 15 requires "different temperature ranges," each corresponding to "groups of performance operating states." LG does not adequately show (*see* Pet. 45 and Table 5) how allegedly the performance states depicted in LG's Table 5 correspond to "detected temperature(s)" or "temperature ranges," as required by independent claims 9 and 15. Indeed, Bhatia is directed to varying a processor's performance state in relation to a target temperature (e.g., T_y *is greater than the target temperature* T_t in Figures 12 and 14). *See e.g.*, Ex. 1006, Abstract (emphasis added), 2:23–27, 9:46–59, 10:7–18; Figs. 12 and 14. Thus, LG does not explain sufficiently how this disclosure anticipates the challenged claims.

Accordingly, we determine that LG has not established a reasonable likelihood of prevailing in showing that independent claims 9 and 15, and, for the same reasons, dependent 10, 13, 14, and 16, are anticipated by Bhatia.

Obviousness

LG contends that claims 17 would have been obvious over Lee. Pet. 56–60. Similar to claims 9 and 15, claim 17 requires "the processor having a plurality of groups of performance states associated with each of a plurality of temperature ranges." LG's analysis of this limitation as having been obvious over Bhatia relies on its anticipation claim chart for claim 9. Pet. 58–59. For the same reasons discussed above as to why LG has not persuaded us sufficiently that Bhatia anticipates claim 9, LG has not persuaded us that claim 17 is obvious over Bhatia.

Accordingly, we determine that LG has not established a reasonable likelihood of prevailing in showing that claim 17 is obvious over Bhatia.

III. CONCLUSION

For the forgoing reasons, we determine, based on the Petition and the accompanying evidence, that there LG has not shown a reasonable likelihood that LG will prevail on any of its challenges to claims 9, 10, 14–17 of the '332 patent.

IV. ORDER

In consideration of the foregoing, it is

ORDERED that the Petition is *denied*, and no trial is instituted.

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