UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

_____

Case IPR2015-00060
Patent 7,421,032 B2

_____

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and
TREVOR M. JEFFERSON, *Administrative Patent Judges*.

PERRY, *Administrative Patent Judge*.

DECISION
Denying *Inter Partes* Review
37 C.F.R. § 42.108

INTRODUCTION

A. Background

Hughes Network Systems, LLC and Hughes Communications, Inc. (collectively "Petitioner") filed a Petition to institute an *inter partes* review of claims 1, 8, 10, 18, 19, and 22 of U.S. Patent No. 7,421,032 B2 ("the '032 patent"). Paper 4 ("Pet.").[1] California Institute of Technology ("Patent Owner") timely filed a Preliminary Response. Paper 13 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons given below, we do not institute an *inter partes* review in this proceeding.

B. Related Proceedings

Petitioner states that the '032 Patent (Ex. 1005) is involved in a pending lawsuit titled *California Institute of Technology v. Hughes Communications, Inc.*, No. 13-CV-07245 (CACD) ("the Lawsuit"). *See* Ex. 1015. The Lawsuit includes the following patents: (i) U.S. Patent No. 7,116,710; (ii) U.S. Patent No. 7,421,032; (iii) U.S. Patent No. 7,916,781; and (iv) U.S. Patent No. 8,284,833.

The '032 patent belongs to a patent family also including U.S. Patent No. 7,116,710, U.S. Patent No. 7,916,781, and U.S. Patent No. 8,284,833, which are the subject of related proceedings including IPR2015-00059, IPR2015-00061, IPR2015-00067, IPR2015-00068, and IPR2015-00081.

---

[1] "Pet." refers to the corrected petition filed October 30, 2014 (Paper 4).

THE '032 PATENT (Ex. 1003)

A. Background and Context

We understand that error correcting codes are used to communicate information across a noisy communication channel. They enable the recovery of a transmitted message that has become distorted by channel noise. To prepare a message for transmission, it is parsed into groups of message bits that are "encoded" into "codewords" by adding redundant information to them.[2] The codewords are transmitted over the communication channel and are received at another location, where the codewords are "decoded" into the original message. No single coding scheme is optimal for all communication channels. Also, there are design tradeoffs between the use of complex codes, which permits better error correction, and less complex codes, which are easier to decode. This has led to the development of many different encoding/decoding schemes. The '781 patent describes one such scheme.
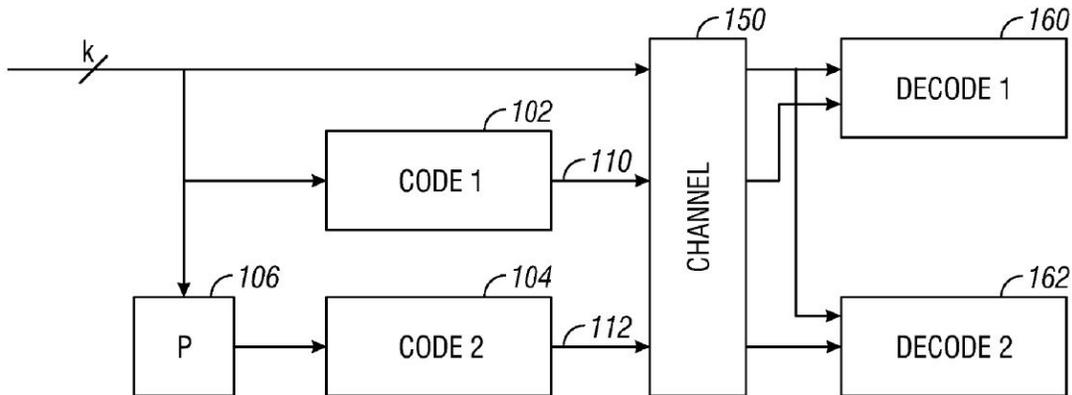
B. The '032 Patent Invention

The '032 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1003, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

---

[2] For example, input message bits "10011" may be encoded into a codeword "100111" by adding a "parity" bit "1" to the original message.

100

FIG. 1
(Prior Art)

Fig. 1 is a schematic diagram of a prior "turbo code" system. Ex. 1003, 2:16–17. The '032 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102, 104 are typically recursive convolutional coders.

> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Ex. 1003, 1:41–56. A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.
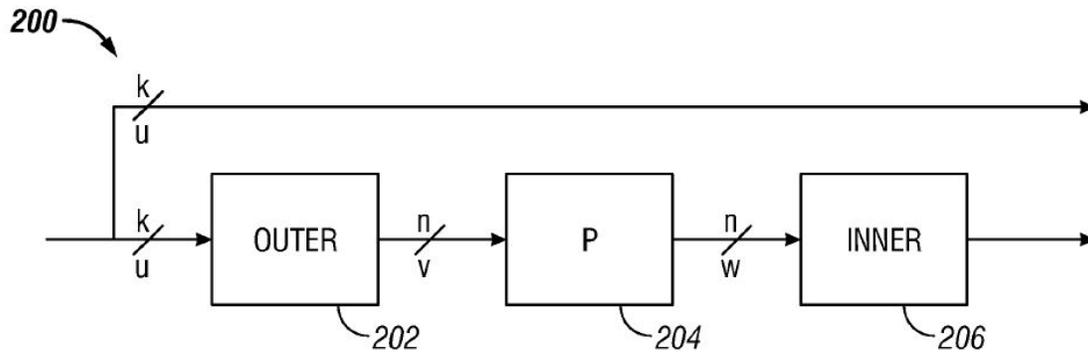
FIG. 2

Figure 2 is a schematic diagram of a coder according to an embodiment.

The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206. . . . The outer coder 202 receives the uncoded data [that] may be partitioned into blocks of fixed size, [e.g.] k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n x k matrix, and the rate[3] of the coder is k/n.

The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence or degree profile, of the code.

The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_iw$, where T_i is a nonsingular n x n matrix. The inner coder 210 can have a

---

[3] The "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits. Ex. 1010 ¶ 19.

5

rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

Ex. 1003, 2:36–65. We understand that codes characterized by a regular repeat of message bits into a resulting codeword are referred to as "regular repeat," whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as "irregular repeat." The second ("inner") encoder 206 performs an "accumulate" function. Thus, the two step encoding process illustrated in Figure 2 including a first encoding ("outer encoding") followed by a second encoding ("inner encoding") results in either a "regular repeat accumulate" ("RRA") code or an "irregular repeat accumulate" ("IRA") code, depending upon whether the repetition in the first (outer) encoding is regular or irregular.

Figure 4 of the '032 patent is reproduced below.
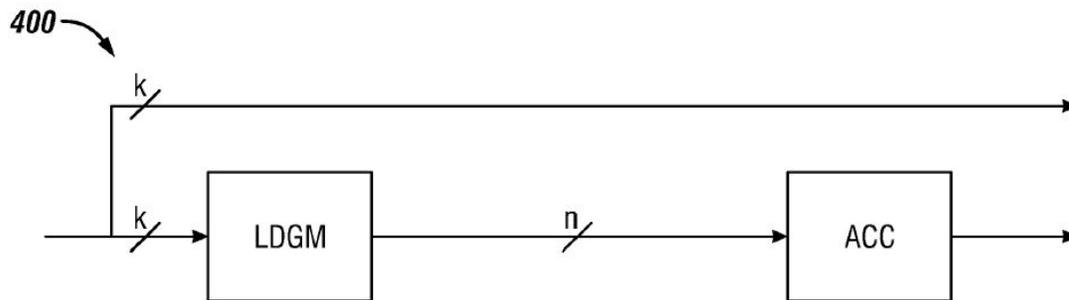
FIG. 4

Figure 4 shows an alternative embodiment in which the first encoding is carried out by a low density generator matrix. Low density generator matrix (LDGM)[4] codes are a special class of low density parity check codes that allow for less encoding and decoding complexity. LDGM codes are

---

[4] We understand that a "generator" matrix (typically referred to by "G") is used to create (generate) codewords. A parity check matrix (typically referred to by "H") is used to decode a received message.

systematic linear codes generated by a "sparse" generator matrix. No
interleaver (as in the Figure 2 embodiment) is required in the Figure 4
embodiment because the LDGM provides scrambling otherwise provided by
the interleaver in the Figure 2 embodiment. Ex. 1003, 3:55–64.

C. Illustrative Claims

Of the claims challenged, independent claim 1 is directed to a method
of encoding. Independent claim 18 is directed to a decoder (device). Both
of these independent claims are illustrative and are reproduced below
(bracketed limitation references added).

1. A method, comprising:

[a] receiving a collection of message bits having a first
sequence in a source data stream;

[b] generating a sequence of parity bits, wherein each parity bit
"x_i" in the sequence is in accordance with the formula

$$x_j = x_{j-1} + \sum_{i=1}^{\lambda} v_{(j-1)\lambda+i},$$

where

"x_{j-1}" is the value of a parity bit "j−1," and

$$\text{"}\sum_{i=1}^{a} v_{(j-1)a+1}\text{"}$$

is the value of a sum of "a" randomly chosen irregular repeats
of the message bits; and

[c] making the sequence of parity bits available for transmission
in a transmission data stream.

18. A device comprising:

[a] a message passing decoder configured to decode a received data stream that includes a collection of parity bits,

[b] the message passing decoder comprising two or more check/variable nodes operating in parallel to receive messages from neighboring check/variable nodes and send updated messages to the neighboring variable/check nodes,

[c] wherein the message passing decoder is configured to decode the received data stream that has been encoded in accordance with the following Tanner graph:
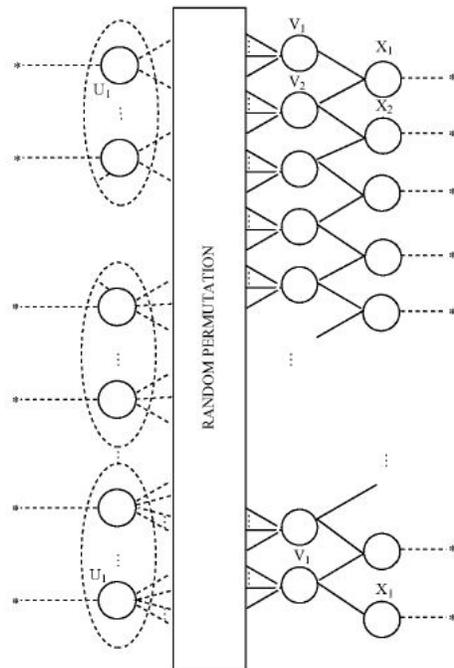
ALLEGED GROUNDS OF UNPATENTABILITY

Petitioner contends that the challenged claims are unpatentable on the following specific grounds.[5]

------

[5] Petitioner supports its challenge with Declaration of Henry D. Pfister, Ph.D. (Ex. 1010, "Pfister Decl.").

Reference(s)	Basis	Claim(s) Challenged
Frey[6] and Divsalar[7]	35 U.S.C. § 103	1
Frey, Divsalar, and Luby[8]	35 U.S.C. § 103	1, 8, and 10
Frey, Divsalar, Luby, and Hall[9]	35 U.S.C. § 103	1, 8, and 10
Frey, Divsalar, and Kschischang[10]	35 U.S.C. § 103	18, 19, and 22
Frey, Divsalar, Kschischang, and Hall	35 U.S.C. § 103	18, 19, and 22
Divsalar and Luby	35 U.S.C. § 103	1 and 8
Divsalar, Luby and Kschischang	35 U.S.C. § 103	18 and 22

---

[6] Brendan J. Frey & David J.C. MacKay, *Irregular Turbocodes*, PROCEEDINGS OF THE 37TH ANNUAL ALLERTON CONFERENCE ON COMMUNICATION, CONTROL, AND COMPUTING, 1999, at 1–7 (Ex. 1012, "Frey").

[7] Divsalar et al., *Coding Theorems for 'Turbo-Like' Codes*, THIRTY-SIXTH ANNUAL ALLERTON CONFERENCE ON COMMUNICATION, CONTROL, AND COMPUTING, Sept. 23–25, 1998, at 201–209 (Ex. 1011, "Divsalar").

[8] U.S. Patent No. 6,081,909, application filed November 6, 1997 (Ex. 1016, "Luby").

[9] Eric K. Hall and Stephen G. Wilson, *Stream-Oriented Turbo Codes*, 48TH IEEE VEHICULAR TECHNOLOGY CONFERENCE, 1998, at 71–74 (Ex. 1013, "Hall").

[10] F. R. Kschischang & B. J. Frey, *Iterative decoding of compound codes by probability propagation in graphical models*, 16 IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS 219–230 (1998) (Ex. 1017, "Kschischang").

Reference(s)	Basis	Claim(s) Challenged
Divsalar, Luby and Ping[11]	35 U.S.C. § 103	10
Divsalar, Luby, Kschischang, and Ping	35 U.S.C. § 103	19

ANALYSIS OF CLAIM CHALLENGES[12]

A. Claim Construction

Claim constructions presented in this Decision are preliminary in that they are based on the record developed thus far, prior to Patent Owner's formal response. Constructions may change as the record more fully develops.

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special

---

[11] Li Ping et al., *Low Density Parity Check Codes with Semi-Random Parity Check Matrix*, 35 IEEE ELECTRONICS LETTERS 38–39 (1999) (Ex. 1014, "Ping").

[12] Patent Owner argues that, as a threshold matter, the Petition should be dismissed because Petitioner fails to identify all real parties in interest. Prelim. Resp. 3. Because we have determined that Petitioner has not demonstrated a reasonable likelihood of prevailing, we need not address the real parties in interest issue in this Decision.

definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

We determine that only the following claim constructions are necessary for the purposes of this decision.

1. *Equation in "generating step" of claim 1*

The equation in the "generating" step of claim 1 refers to the following equation:

$$x_j = x_{j-1} + \sum_{i=1}^{\lambda} v_{(j-1)\lambda+i},$$

where

"x_{j-1}" is the value of a parity bit "$j-1$," and

$$\text{``}\sum_{i=1}^{a} v_{(j-1)a+1}\text{''}$$

.

Petitioner construes the equation in the "generating" step to mean: "the parity bit x_j is the sum of (a) the parity bit x_{j-1} and (b) the sum of a number, 'a' of randomly chosen irregular repeats of the message bits." Pet. 12. We adopt Petitioner's construction with the following further explanation. A parity bit x_j is determined by two components. The first component is the parity bit previous to the parity bit being determined (parity bit x_{j-1}). The second component is the sum of "a" ("a" is a number) message bits (information bits) that have been randomly repeated.

2. *"irregular" (claim 1 generating step)*

Petitioner proposes a construction of "irregular" as: "a different

number of times." Pet. 13. However, Petitioner refers, in its Petition in a related case, to testimony of Dr. Pfister that explains that "irregular" in the context of error correcting codes means that different message bits contribute to different numbers of parity bits. *Hughes Network Sys., Inc. v. Cal. Inst. of Tech.*, Case IPR2015-00059, Paper 4, at 7 (PTAB Oct. 30, 2014) (Petition, citing accompanying Ex. 1010 ¶¶ 28–29, 33). In the context of the '032 patent specification, we adopt the construction: "irregular" refers to the notion that different message bits or groups of message bits contribute to different numbers of parity bits.

3. Tanner Graph (claim 18)

The following Tanner graph appears in claim 18.
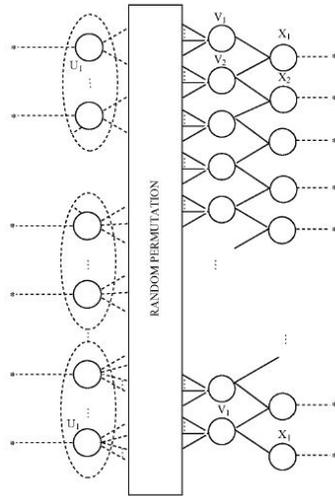
It corresponds to '032 patent Figure 3, reproduced below, which includes reference characters that render it more easily understood and explained.
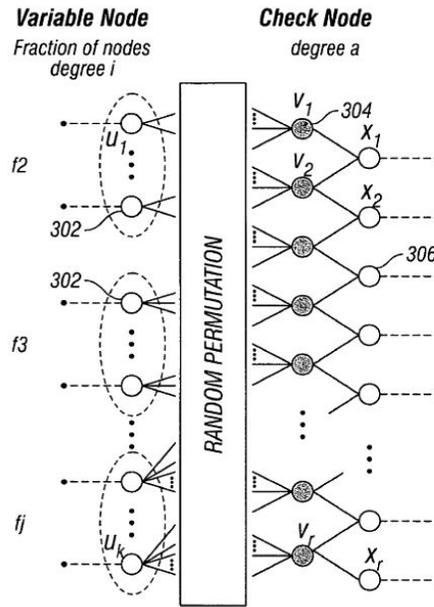
FIG. 3

Figure 3 is described as a Tanner graph for an irregular repeat and accumulate (IRA) coder. The left-most column of nodes 302 are variable nodes that receive information bits. The column of nodes just to the right of the "RANDOM PERMUTATION" block are check nodes v indicated by reference numeral 304. An information bit node connected to two check nodes represents a repeat = 2. An information node connected to three check nodes represents a repeat = 3. The nodes in the right-most column are parity bit nodes x, referenced by 306. As shown by the edges[13] of the Tanner graph, each parity bit is a function of its previous parity bit and is also a function of information bits (edges connect through check nodes and random permutation to information bit nodes). Ex. 1003, 3:34–55. Petitioner proposes a construction of the Tanner graph as follows:

---

[13] We understand that "edges" are the straight lines that connect one node to another node of a Tanner graph.

> a graph representing an [irregular repeat accumulate] IRA code
> as a set of parity checks where every message bit is repeated, at
> least two different subsets of message bits are repeated a
> different number of times, and check nodes, randomly
> connected to the repeated message bits, enforce constraints that
> determine the parity bits.

Pet. 14 (citing Ex. 1024, 22–23). Patent Owner does not propose a construction.

Petitioner's construction, while accurate, does not fully explain edges that connect two parity bit nodes via a check node. These edges make each parity bit a function of other parity bits (in addition to being a function of information bits). We, therefore, adopt Petitioner's construction narrowed by the added constraint that a parity bit is determined as a function of both information bits and other parity bits as shown by the configuration of nodes and edges of the Tanner graph.

B. Frey (Ex. 1012)

Patent Owner challenges the availability of Frey as a publication reference against the challenged claims. Prelim. Resp. 20–23.

Petitioner asserts that Frey was published "no later than October 8, 1999." Pet. iii. Without explanation in the Petition, Petitioner directs us to a Declaration by Dr. David J.C. MacKay, who indicates that the asserted publication date is based on his own recollection of events about 15 years ago. Pet. 2 (citing Ex. 1060 ("MacKay Decl.") ¶ 44).

Patent Owner argues that Petitioner's failure to discuss the publication date in the body of the Petition itself amounts to Petitioner circumventing the page limits set by our rules. Prelim. Resp. 21.

While we appreciate the historical tutorial of the development of codes provided by Dr. MacKay's Declaration, in excess of forty paragraphs,

it does not provide sufficient corroboration that the Frey paper was actually published no later than a particular date that he now recalls 15 years later.

The Frey document appears from its first page to be a paper prepared for the 37th Allerton Conference, which occurred in 1999. However, the first page does not bear any of the indicia normally found on an Allerton Conference paper, such as on the cover page of Divsalar.
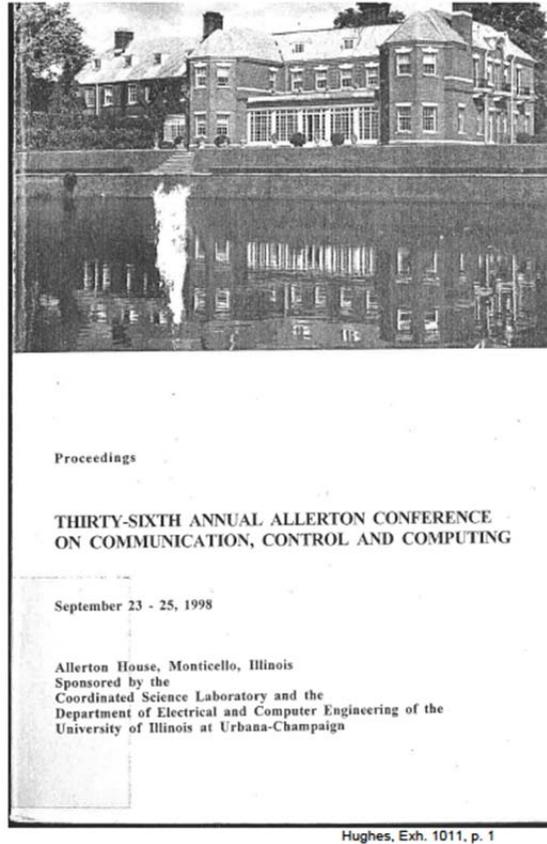
Also, Dr. David J.C. MacKay is a co-author (with Frey) of the paper. Dr. MacKay's Declaration, however, is silent as to whether the paper at issue was actually presented at the 37th Allerton Conference. He states only that collaboration resulted in a "presentation" at Allerton. Furthermore, there is no confirmation by receipt at a recognized library after the conference.

Based on this record, we find that Frey is not a publication available for challenging the claims of the '032 patent. Because we do not consider Frey to be available as a publication reference against the '032 patent, we decline to grant the Petition as to grounds relying on Frey.

C. Divsalar (Ex. 1011)

1. Divsalar as a Publication

Divsalar stands in a different position from Frey. The cover page of the Divsalar document is reproduced below.

Proceedings

THIRTY-SIXTH ANNUAL ALLERTON CONFERENCE
ON COMMUNICATION, CONTROL AND COMPUTING

September 23 - 25, 1998

Allerton House, Monticello, Illinois
Sponsored by the
Coordinated Science Laboratory and the
Department of Electrical and Computer Engineering of the
University of Illinois at Urbana-Champaign

Hughes, Exh. 1011, p. 1

The cover page includes a photograph of the "Allerton House" in which the Allerton Conference is held. It also includes the date range of the conference and indicates sponsorship information.

Petitioner states that Divsalar was "published no later than April 30, 1999 at the University of Texas library." Pet. iii. In support, Petitioner proffers the declaration testimony of the University of Texas librarian (Ex. 1064), including an acquisition record pasted into an email. According to Pfister (Petitioner's declarant), the Allerton Conference is generally regarded as one of the main conferences in the field of information theory and communications. Ex. 1010 ¶ 29.

Patent Owner argues that Petitioner has not established that Divsalar is a printed publication within the meaning of § 311(b). Patent Owner states that the acquisition record of the University of Texas library does not state

16

that the paper was actually shelved or otherwise displayed and accessible to those of "ordinary skill." Prelim. Resp. 24–25.

According to the Divsalar cover page, it was presented at the Allerton Conference held on September 23–25, 1998. Ex. 1011, 1. The acquisition record of the University of Texas indicating acquisition in April 1999 lends credence to the actual presentation of the paper at the September 1998 Allerton Conference. *See* Ex. 1064 (attachment to Declaration of Robin Fradenburgh). Given, Dr. Pfister's testimony that the Allerton Conference is the premier conference for information theorists, we find sufficient evidence to establish Divsalar as a printed publication within the meaning of § 311(b).

We note that Divsalar is listed as being of record among the "References Cited" in U.S. Patent No. 7,916,781 (IPR2015-00059). It was cited by the Applicant in an IDS apparently filed with the application on June 30, 2008.

On this record, we therefore consider Divsalar to be a printed publication reference available to challenge the claims of the '032 patent. .

2. *What Divsalar describes*

Divsalar discloses "turbo-like" coding systems that are built from fixed convolutional codes interconnected with random interleavers, including both parallel concatenated convolutional codes and serial concatenated convolutional codes as special cases. Ex. 1011, 3.[14] With fixed component codes and interconnection topology, Divsalar demonstrates that as the block length approaches infinity, the ensemble (over all possible interleaves) maximum likelihood error probability approaches zero, if the

---

[14] Ex. 1011 includes page numbers indicated by the publication itself, and different page numbers provided by Petitioner. Our references are to the page numbers provided by Petitioner.

ratio of energy per bit to noise power spectral density exceeds some

threshold. *Id.*

The general class of concatenated coding systems is depicted in

Figure 1 of Divsalar, as follows:
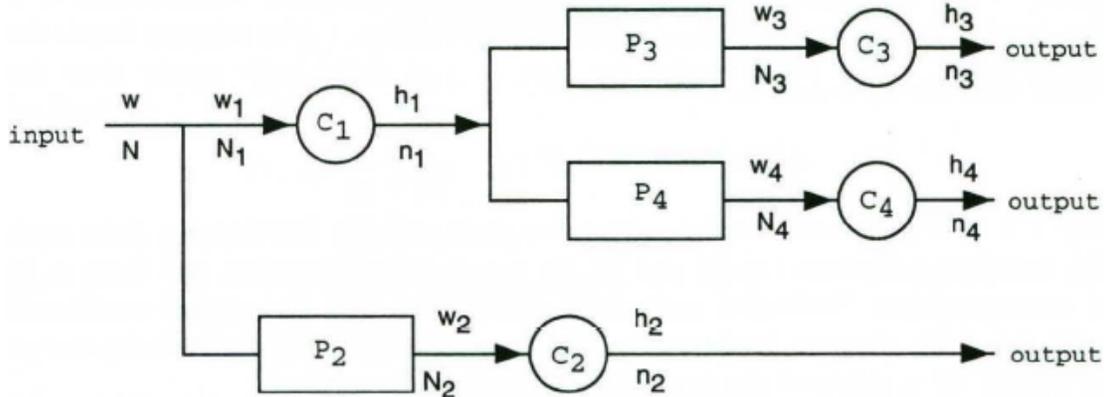
Figure 1. A "turbo-like" code with
$s_I = \{1, 2\}$, $s_O = \{2, 3, 4\}$, $\bar{s}_O = \{1\}$.

Figure 1 illustrates that encoders C_2, C_3, and C_4 are preceded by

interleavers (permuters) P_2, P_3, and P_4, except C_1, which is connected to an

input rather than an interleaver. *Id.* at 4. The overall structure must have no

loops and, therefore, is called a "turbo-like" code. *Id.*

Divsalar further discloses that "turbo-like" codes are repeat and

accumulate ("RA") codes. *Id.* at 7. The general scheme is depicted in

Figure 3 as follows:
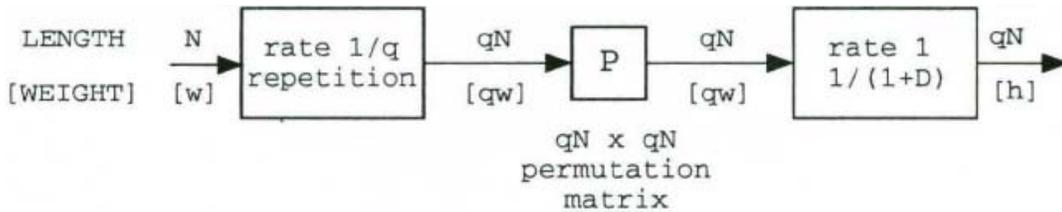
Figure 3. Encoder for a (qN, N) repeat and accumulate
code. The numbers above the input-output lines
indicate the length of the corresponding block, and
those below the lines indicate the weight of the block.

Figure 3 illustrates that information block of length N is repeated q

times, scrambled by interleaver of size qN, and then encoded by a rate1

accumulator. *Id.* The accumulator can be viewed as a truncated rate-1

recursive convolutional encoder. *Id.* Figure 3 further illustrates a simple

class of rate 1/q serially concatenated codes where the outer code is a q-fold

repetition code and the inner code is a rate-1 convolutional code with a

transfer function 1/(1+ D). *Id.*

D. Divsalar and Luby (claims 1 and 8)

According to Petitioner, Divsalar describes two stages of encoding

with the second being rate = 1. Pet. 45. We agree. Petitioner acknowledges

that bits accumulated by the rate = 1 accumulator are not "randomly chosen

irregular repeats of the message bits." *Id.* Petitioner relies upon Luby as

describing an "irregular graphing" encoder that provides "randomly chosen

irregular repeats of the message bits." *Id.* According to Petitioner, this is

demonstrated by Luby's Figure 17, reproduced below.
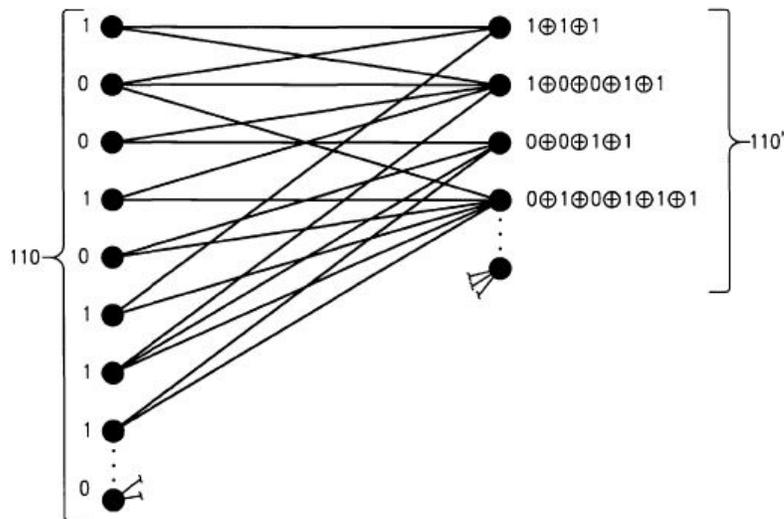
FIG. 17

Luby's Figure 17 depicts an irregular graphing of the edges between

node layers in the Figure 16 encoding structure. Ex. 1016, 5:44–46.

According to Petitioner, the circles (nodes) in the left column represent information bits to be encoded, and the circles (nodes) in the right column represent parity bits computed from the information bits. Pet. 45 (citing Ex. 1010 ¶ 193). Each parity bit on the right is computed by summing together (modulo 2) all of the information bits connected to that parity bits by an edge.[15] *Id*.

According to Petitioner, if d_i is the degree (or the number of adjacent edges) of the i-th information bit, then some information bits are connected to two parity bits (i.e., have a degree of two) and other information bits are connected to three parity bits (i.e., have a degree of three). *Id*. Further, according to Petitioner, Luby discloses that the number of edges assigned to a data bit is randomly chosen, as reproduced above. Pet. 45 (citing Ex. 1016, 4:55–67; Ex. 1010 ¶ 194). Petitioner argues that a person of ordinary skill in the art would understand that Luby's assignment of edges to the data bits is within the broadest reasonable interpretation of the equation of claim 1 where there are 'a' randomly chosen irregular repeats of the message bits." *Id*. ¶ 195.

According to Dr. Pfister, Luby's Figure 17 describes the functional relationship between the information bits and the parity bits. There are two ways that the graph can compute the parity bits from the information bits. Ex. 1010 ¶ 196. In the first way, the information bits pass their values to the attached checks. *Id*. In this case, the i-th information bits repeat its value d_i times. *Id*. The second approach is to sequentially compute the value of each parity-check bit. In the second approach, a parity bit can be seen to request bit values from each of its attached information bit nodes. *Id*. Thus,

---

[15] The "edges" are the straight lines connecting nodes in the left column with nodes in the right column.

the i-th information bit receives d_i requests and is, hence, repeated d_i times in the computation. Pet. 46 (citing Ex. 1010 ¶¶ 196–198. According to Dr. Pfister, Luby meets the broadest reasonable interpretation of "a number, 'a' of randomly chosen irregular repeats of the message bits." *Id.* ¶¶ 196–198.

Petitioner argues that one of ordinary skill would have been motivated to combine Divsalar and Luby. Pet. 47–49. Patent Owner, however, points out a flaw in Petitioner's reasoning. According to Petitioner's own claim construction, the equation of element 1[b] requires that "the parity bit x_j is the sum of (a) the parity bit x_{j-1} [the previous parity bit] and (b) the sum of a number, 'a,' of randomly chosen irregular repeats of the message bits." *Id.* at 12–13. According to Petitioner's description of Luby, there is no sum taken that includes both information bits and the *previous parity bit* as claim 1 requires. *Seesupra* section A.1.

Petitioner's declarant states the parity bits disclosed in Luby are computed by "summing together (modulo 2) all of the information bits connected to that parity bits [sic] by an edge in the graph." *Id.* at 45; *see* Ex. 1010 ¶ 193. Patent Owner correctly notes, however, that Luby does not describe a parity bit being computed by summing information bits and another parity bit. Pet. 54. This is evidenced, for example, by Figure 17 of Luby, above, which shows no edges connecting parity bit nodes. *Id.*

Because Luby does not describe what is required by the equation of claim 1, we conclude that Petitioner has not demonstrated a reasonable likelihood of succeeding with this challenge.

E. Divsalar, Luby and Kschischang (claims 18 and 22)

Independent claim 18 describes a decoder for reconstructing a

message that was encoded per the Tanner graph in claim 18 and then transmitted through a communication channel.

Petitioner reads claims 18 and 22 on Divsalar, Luby, and Kschischang. Pet. 49–53. Petitioner relies upon Kschischang as describing how to build a message-passing decoder that is "operating in parallel to receive messages from neighboring check/variable nodes and send updated messages to the neighboring variable/check nodes." Pet. 37 (citing Ex. 1010 ¶ 124). Petitioner also relies upon Kschischang as teaching that an irregular repeat-accumulation may be represented by a Tanner graph. Pet. 52.

Petitioner relies on Luby's Figure 17 as describing requirements of the Tanner graph in claim 18. Pet. 51. We construed the Tanner graph of claim 18 limitation (c) as requiring a parity bit to be dependent not only on information bits, but also on a previous parity bit (connected by an edge in the Tanner graph). However, Luby's Figure 17 does not demonstrate dependence of a parity bit on any other parity bit, as claimed. Rather, it demonstrates only that parity bits only are dependent on variable repeats of information bits.

It is, therefore, not reasonably likely that Petitioner will succeed in this challenge. We reach the same result for claim 22 depending from claim 18.

F. Divsalar, Luby, and Ping (claim 10)

Claim 10 depends from claim 8, which depends from claim 1. For the same reasons stated with respect to claim 1, the Divsalar and Luby combination fails.

Ping discloses a semi-random approach to low density parity check ("LDPC") code design that achieves essentially the same performance as an

existing method, but with considerably reduced complexity. Ex. 1014, 6.[16]

An LDPC code is defined by a randomly generated parity check matrix H. Ping utilizes a semi-random technique, where only H is generated randomly, and the remaining part is deterministic. *Id.* Codeword c is decomposed to $c = [p, d]^t$, where p and d contain the parity bits and information bits. *Id.* Accordingly, H is decomposed to $H = [H^p, H^d]$. H^p is constructed in a deterministic form. *Id.* H^d is partitioned in to *t* equal sub-blocks, where *t* is constrained by *n–k / t* and *kt / n–k* (where *n–k* are the number of rows). *Id.* In each sub-block, one element is randomly created 1 per column and *kt/(n–k)* 1s per row. *Id.* The resultant H^d has a column weight of t and a row weight of *kt/(n–k)*. *Id.*

This method is much simpler than a full Gaussian elimination. Furthermore, a random H^d can be singular, causing additional programming complexity in realizing a specified rate. Even further, there is a memory saving because it requires little memory to store H^d in the encoder if H^d is sparse. *Id.*

There is no teaching in Ping that supplements sufficiently the deficiency noted with respect to Luby above.

G. *Divsalar, Luby, Kschischang, and Ping (claim 19)*

Claim 19 depends from claim 18. For the same reasons stated with respect to claim 18, the Divsalar and Luby combination fails. Neither Kschischang nor Ping supplements sufficiently the deficiency noted with respect to Luby above.

---

[16] Ex. 1014 includes page numbers indicated by the publication itself, and different page numbers provided by Petitioner. Our references are to the page numbers provided by Petitioner.

SUMMARY

For the foregoing reasons, we determine that the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail on at least one alleged ground of unpatentability with respect to claims of the '032 patent.

ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby denied as to all grounds raised in the Petition for the reasons stated above.

PETITIONER:

Eliot D. Williams
G. Hopkins Guy
Baker Botts, LLP
eliot.williams@bakerbotts.com
hop.guy@bakerbotts.com

PATENT OWNER:

Michael T. Rosato
Matthew A. Argenti
Wilson Sonsini Goodrich & Rosati
mrosato@wsgr.com
margenti@wsgr.com