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Paper 8
Entered: November 21, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANON INC.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2014-00757
Case IPR2014-00952[1]
Patent 8,300,285 B2

Before THOMAS L. GIANNETTI, JAMES A. TARTAL, and PATRICK M. BOUCHER, *Administrative Patent Judges*.

BOUCHER, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review in IPR2014-00757 and
Denying Institution of *Inter Partes* Review in IPR2014-00952
37 C.F.R. § 42.108

[1] This paper addresses issues in the above-listed cases. The parties are not authorized to use this heading style for any subsequent papers.

On May 15, 2014, Canon Inc. ("Petitioner") filed a Petition (Paper 1 of IPR2014-00757, "Pet. 757") pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–20 of U.S. Patent No. 8,300,285 ("the '285 patent"). Intellectual Ventures I LLC ("Patent Owner") filed a Preliminary Response (Paper 6 of IPR2014-00757, "Prelim. Resp. 757") on August 28, 2014. On June 13, 2014, Petitioner filed a Petition (Paper 1 of IPR2014-00952, "Pet. 952") to institute an *inter partes* review of the same claims of the '285 patent, and Patent Owner filed a Preliminary Response (Paper 6 of IPR2014-00952, "Prelim. Resp. 952") on September 24, 2014. Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we institute an *inter partes* review of claims 1–20. The Board has not made a final determination of the patentability of any claim.

I. BACKGROUND

A. The '285 Patent (Ex. 1001)

The '285 patent is a continuation of U.S. Patent No. 7,315,406 ("the '406 patent"), which is the subject of *Canon Inc. v. Intellectual Ventures I LLC*, Case IPR2014-00535 (PTAB), a proceeding in which we instituted *inter partes* review on September 24, 2014. The '285 patent describes scanning circuit structures for scanners capable of reducing distortion during

high-speed image signal transmission. Ex. 1001,[2] col. 2, ll. 9–14. Figure 2 of the '285 patent is reproduced below.

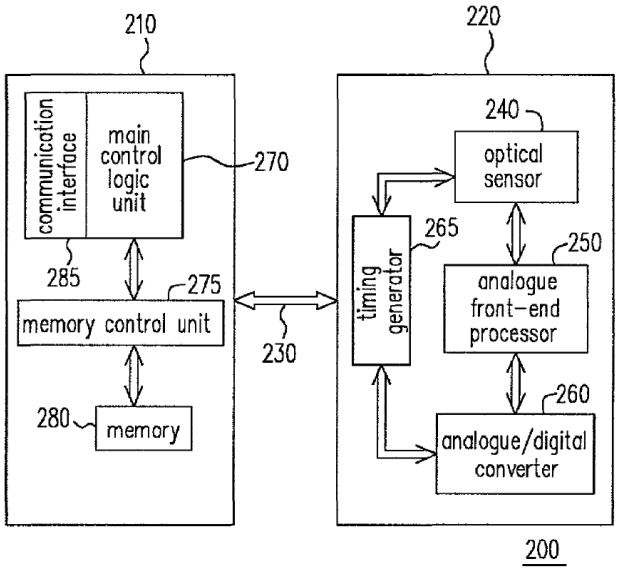

Figure 2 illustrates a circuit structure for a scanner, including main circuit module 210 and optical sensor circuit module 220 linked together with flat cable 230. *Id.* at col. 3, ll. 39–43. Communication interface 285 of the main circuit module allows interfacing with a human being, such as over a universal serial bus ("USB") interface. *Id.* at col. 3, ll. 50–59. The communication interface receives scanning instructions regarding image resolution, brightness level, and scanning range, and converts such scanning instructions into scanning control signals that are conveyed to the optical sensor circuit module over the flat cable. *Id.* Timing generator 265 produces timing control signals for extracting an analog signal image from

[2] Petitioner designates exhibits filed in IPR2014-00757 as Ex. **10**XX and exhibits filed in IPR2014-00952 as Ex. **11**XX. Unless necessary for clarity, when the same exhibit has been filed in both proceedings, we cite to the exhibit filed in IPR2014-00757.

optical sensor 240, which may be a charge-coupled device ("CCD") or complementary metal-oxide-semiconductor ("CMOS") image sensor. *Id.* at col. 3, ll. 60–66. After preprocessing of a collected image by analog front-end preprocessor 250, analog/digital converter 260 ("A/D converter") converts the preprocessed image to digital data, which are transmitted to the main circuit module over the flat cable. *Id.* at col. 3, l. 65 – col. 4, l. 4.

The '285 patent identifies two specific advantages of this arrangement. First, a clearer image can be obtained at higher scanning speeds because the flat cable transmits digital data instead of easily distorted analog image signals. *Id.* at col. 4, ll. 25–27. Second, electromagnetic-interference effects are mitigated because the flat cable transmits scanning control signals rather than timing control signals. *Id.* at col. 4, ll. 28–31.

B. Illustrative Claim

Claim 7 of the '285 patent is illustrative of the claims at issue:

> 7. An apparatus, comprising:
>
> a main circuit module;
>
> a connection cable; and
>
> an optical sensor circuit module coupled to the main circuit module through the connection cable, wherein the optical sensor circuit module is configured to:
>
> receive scan control signals from the main circuit module; and
>
> generate timing control signals for extracting an analog image signal in response to the received scan control signals, wherein the received scan control signals do not comprise any timing control signals.

C. Related Proceedings

Petitioner states that Patent Owner has asserted the '285 patent against Petitioner in *Intellectual Ventures I LLC v. Canon Inc.*, 13-cv-473-SLR (D. Del.). Pet. 757, 4; Pet3 952, 1.

D. Claim Construction

The Board interprets claims using the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

1. "scanning instruction"

We agree with Patent Owner that Petitioner's proposed construction of "scanning instruction" as "an instruction related to performing document scanning" (Pet. 757, 6; Pet. 952, 3) improperly introduces extraneous terms. Prelim. Resp. 757, 5; Prelim. Resp. 952, 5. We construe "scanning instruction" in accordance with its plain meaning of "an instruction for scanning." *See* Ex. 1001, col. 3, ll. 55–59.

2. "scan control signals"

We agree with Patent Owner that Petitioner's proposed construction of "scan control signals" as "an intermediary signal based on the scanning instruction" (Pet. 757, 6–7; Pet. 952, 3) improperly introduces extraneous terms. Prelim. Resp. 757, 5; Prelim. Resp. 952, 5. We construe "scan

control signals" in accordance with its plain meaning of "signals for scan control." *See* Ex. 1001, col. 2, ll. 20–22.

3. "timing control signals"

Petitioner proposes that "timing control signals" be construed as "signals generated by a timing generator and used to control the timing of extraction of an analog image signal." Pet. 757, 7; Pet. 952, 3–4. Patent Owner proposes a construction of "signals for timing control." Prelim. Resp. 5–7; Prelim. Resp. 952, 5–7.

In construing "timing control signals" for purposes of this decision, we are mindful that the phrase appears in the claims as part of a negative limitation, namely that "received scan control signals *do not* comprise any timing control signals" (emphasis added). Patent Owner's proposed construction does not correspond to the broadest reasonable construction of the *claims* because its broad proposed construction of "timing control signals" results in a *narrowed* construction of the overall claims.

Petitioner's proposed construction is consistent with the specification. *See* Ex. 1001, col. 3, ll. 61–64 ("the timing generator produces the required timing control signals for extracting an analog image signal from the optical sensor") (reference numbers omitted). Petitioner's proposed construction is also consistent with Patent Owner's acknowledgment during prosecution that clock signals can be timing control signals. Ex. 1011, 9.

For purposes of this decision, we adopt Petitioner's proposed construction of "timing control signals" as "signals generated by a timing

generator and used to control the timing of extraction of an analog image signal."

4. Means-Plus-Function Limitations

Claims 1, 2, and 4–6 include several terms recited as "means for" performing identified functions, which are presumptively construed under 35 U.S.C. § 112, ¶ 6.[3] Both parties identify corresponding structure disclosed in the '285 patent for performing the recited functions, implicitly acknowledging that construction under § 112, ¶ 6, is appropriate. Pet. 757, 7–8; Pet. 952, 4–5; Prelim. Resp. 757, 7–10; Prelim. Resp. 952, 7–10. In most instances, the parties agree in their identifications of such structure, although we agree with Patent Owner's contention that Petitioner's identification is overly narrow for certain terms. Prelim. Resp. 757, 7–10; Prelim. Resp. 952, 7–10. Accordingly, we construe the various means-plus-function limitations with the following correspondence of structure disclosed in the '285 patent.

"means for . . ."	Corresponding structure
"communication means for receiving scan control signals"	connection cable 230
". . . generating timing control signals"	timing signal generator 265

[3] Section 4(c) of the Leahy-Smith America Invents Act ("AIA") re-designated 35 U.S.C. § 112, ¶ 6, as 35 U.S.C. § 112(f). Pub. L. No. 112-29, 125 Stat. 284, 296 (2011). Because the '285 patent has a filing date before September 16, 2012 (effective date), we refer to the pre-AIA version of § 112.

"means for . . ."	Corresponding structure
". . . receiving a scanning instruction from a communication interface"	main circuit module 210, main control logic unit 270, or communication interface 285
". . . producing the scan control signals"	main control logic unit 270, main circuit module 210, or communication interface 285
". . . converting the analog image signal into digital image data"	analog/digital converter 260
". . . extracting the analog image signal"	optical sensor circuit module 220 and optical sensor 240
". . . generating the analog image signal"	optical sensor 240
". . . pre-processing the analog image signal"	analog front-end preprocessor 250
". . . converting the . . . analog image signal into the digital image data"	analog/digital converter 260

E. References

Petitioner relies on the following references.[4]

Hayashi	JP H11-041389	Feb. 12, 1999	Exs. 1004, 1104
Tsuboi	JP H11-046302	Feb. 16, 1999	Ex. 1005
Wada	JP 2000-244716	Sept. 8, 2000	Exs. 1006, 1106
Shiraishi	JP H11-205556	July 30, 1999	Exs. 1007, 1107
Kono	US 6,958,830 B2	Oct. 25, 2005	Exs. 1008, 1108
Ochiai	US 5,457,544	Oct. 10, 1995	Ex. 1009
Kitani	JP 2000-358139	Dec. 26, 2000	Ex. 1105

[4] Petitioner also cites US 5,684,601 (Ex. 1109, "Endo") and US 6,686,958 B1 (Ex. 1112, "Watanabe") in IPR2014-00952, but does not advance any ground of challenge that applies those references.

F. Asserted Grounds of Unpatentability

1. IPR2014-00757

Petitioner challenges claims 1–20 of the '285 patent on the following grounds in IPR2014-00757. Pet. 757, 5–6.

Reference(s)	Basis	Claim(s) Challenged
Hayashi	§ 102(b)	1, 5, 7, 11, 13, 17, and 18
Hayashi and Shiraishi	§ 103(a)	2–4, 8, and 14–16
Hayashi and Kono	§ 103(a)	6, 12, 19, and 20
Hayashi, Shiraishi, and Ochiai[5]	§ 103(a)	9 and 10
Tsuboi and Wada	§ 103(a)	1–7, 11–14, and 16–20
Tsuboi, Wada, and Shiraishi	§ 103(a)	8 and 15
Tsuboi, Wada, Shiraishi, and Ochiai	§ 103(a)	9 and 10

2. IPR2014-00952

Petitioner challenges claims 1–20 of the '285 patent on the following grounds in IPR2014-00952. Pet. 952, 2.

Reference(s)	Basis	Claim(s) Challenged
Hayashi	§ 102(b)	1, 5, 7, 11, 13, 17, and 18
Hayashi and Kitani	§ 103(a)	2–4, 8–10, and 14–16
Hayashi and Kono	§ 103(a)	6, 12, 19, and 20

II. ANALYSIS

A. Asserted Grounds Based on Hayashi

As Patent Owner observes, Petitioner's challenge of claims 1, 5, 7, 11, 13, 17, and 18 as anticipated by Hayashi and its challenge of claims 6, 12,

[5] The Petition for IPR2014-00757 asserts at page 5 that this challenge is based on Hayashi, Shiraishi, and *Kono*, but the explanation of the challenge at pages 38–41 applies Hayashi, Shiraishi, and *Ochiai*. We presume that the statement at page 5 is in error.

19, and 20 as obvious over Hayashi and Kono are substantially duplicated in the two Petitions. *See* Prelim. Resp. 952, 17–18. Petitioner offers no explanation or justification for such duplication. We treat the challenges based on Hayashi alone or in combination with Kono together.[6]

1. Hayashi

Hayashi describes an image-processing device. Ex. 1004 ¶ 1. Figure 1 of Hayashi is reproduced below.

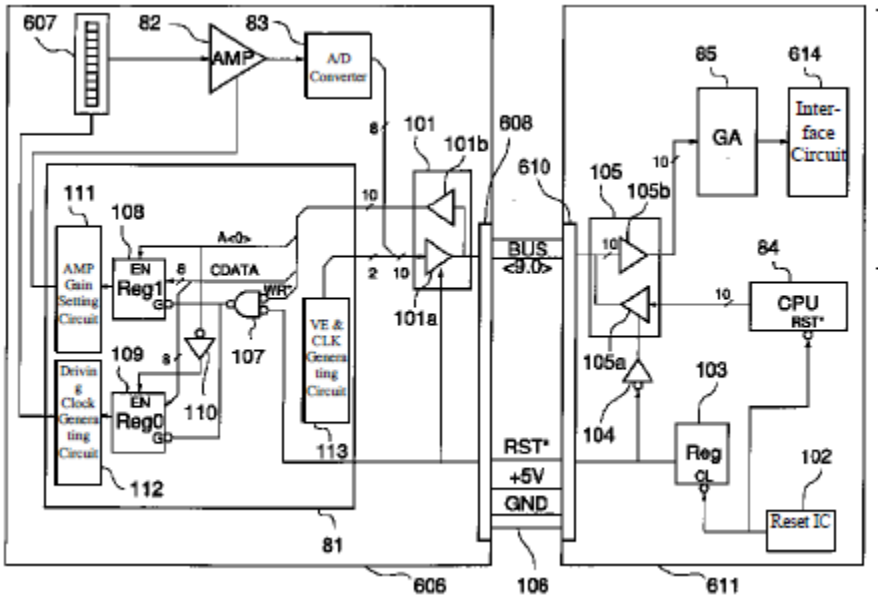

Figure 1 illustrates a structure for a scanner separated into two components joined by scanning cable 106: image processing substrate 611 and reading substrate 606 that includes an image sensor. *Id.* ¶ 3. Image processing substrate 611 includes a CPU that provides overall control of the scanner. *Id.* ¶ 8. When an operator initiates a scanning operation, the CPU outputs a

[6] Patent Owner's response to these challenges is found in its Preliminary Response in IPR2014-00952.

set of signals identified by Hayashi as WR*, A<0>, and CDATA<7, . . . ,0>.[7] *Id.* ¶ 13. The set of signals collectively include ten bits: signal CDATA<7, . . . ,0> is an eight-bit data bus, *id.* ¶ 13; signal A<0> is the least significant bit of a 16-bit address bus, *id.* ¶ 13; and signal WR* is a one-bit writing signal, *id.* ¶ 35.

After originating at CPU 84, the set of signals passes into bidirectional buffer 105 of image processing substrate 611, through connector 610, across scanning cable 106, through connector 608, and into bidirectional buffer 101. The signals then pass to different circuitry components. Of particular relevance, signal A<0> passes to register 109 through inverter 110 so that the inverted digital value of A<0> is input to enable terminal EN of register 109. *Id.* ¶ 37. In addition, signal CDATA<7, . . . ,0> provides 8-bit operating-mode data that are written to register 109. *Id.* ¶ 13. The output of register 109, which depends on values of A<0> and CDATA<7, . . . ,0>, is input into driving clock generating circuit 112 to set the driving mode of the image sensor. *Id.* ¶ 39. Signals generated by driving clock generating circuit 112 drive image sensor 607 and extract analog image data. *Id.* ¶ 40.

2. Anticipation of Claims 1, 5, 7, 11, 13, 17, and 18 by Hayashi

Petitioner challenges claims 1, 5, 7, 11, 13, 17, and 18 as anticipated by Hayashi. Pet. 757, 17–26; Pet. 952, 14–25. Each of independent claims 1, 7, and 13 of the ’285 patent recites the generation of timing control

[7] Reference in ¶ 13 of Petitioner’s English translation of Hayashi to “CDATA<7, . . . , ***60***>” (emphasis added) appears to be an error, as evident from a comparison with the original Japanese version of the same paragraph.

signals in response to receipt of scan control signals, "wherein the [received] scan control signals do not comprise any timing control signals." Petitioner contends that all limitations of the independent claims, including this recitation, are disclosed by Hayashi. Pet. 757, 17–25; Pet. 952, 14–25.

Specifically, Petitioner contends that the set of signals WR*, A<0>, and CDATA<7, . . . ,0> are "scan control signals inasmuch as they are signals that control document scanning." Pet. 952, 15; *see* Pet. 757, 17. Petitioner also contends that signals output by driving clock generating circuit 112 are "timing control signals." Pet. 757, 18; Pet. 952, 16. Patent Owner does not contest these positions.

Petitioner additionally identifies a distinction in the functionality of signals WR*, A<0>, and CDATA<7, . . . ,0> and the functionality of signals output by driving clock generating circuit 112. Because the signals output by the driving clock generating circuit are produced *in response to* a data value carried by CDATA<7, . . . ,0>, Petitioner contends that CDATA<7, . . . ,0> is not itself a timing control signal. Pet. 757, 19; Pet. 952, 17. Noting Patent Owner's acknowledgment during prosecution of the '285 patent that clock signals are timing control signals, Petitioner reasons that only signals output by Hayashi's driving clock generating circuit are timing control signals and not signals traveling *to* the driving clock generating circuit. Pet. 757, 19; Pet. 952, 17. We are persuaded that Petitioner has made an adequate showing.

Patent Owner responds that at least signals A<0> and CDATA<7, . . . ,0> control Hayashi's driving clock, noting that Petitioner acknowledges such control by CDATA<7, . . . ,0>. Prelim. Resp. 952, 22–

23. Patent Owner contends that such signals are, therefore, also "timing control signals." *Id.* Patent Owner's argument relies critically on its broad construction of "timing control signals." As explained *supra*, we reject that construction for purposes of this decision because it does not correspond to the broadest reasonable interpretation of the claims.

We conclude that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to independent claims 1, 7, and 13 as anticipated by Hayashi. We have also reviewed Petitioner's claim charts for dependent claims 5, 11, 17, and 18 (Pet. 757, 21–26; Pet. 952, 20–25), and conclude that Petitioner has also demonstrated a reasonable likelihood of prevailing on its challenge to those claims as anticipated by Hayashi.

Accordingly, we institute *inter partes* review in IPR2014-00757 of claims 1, 5, 7, 11, 13, 17, and 18 as anticipated by Hayashi under 35 U.S.C. § 102(b). Furthermore, because the same claims are challenged on the same ground in IPR2014-00952, we decline also to institute a second *inter partes* review of the claims on that ground.[8] *See* 35 U.S.C. § 325(d); 37 C.F.R. § 42.108(b).

[8] We recognize that in instituting *inter partes* review in IPR2014-00757, but not in IPR2014-00952, Patent Owner's argument that signals A<0> and CDATA<7, . . . ,0> are timing control signals is not of record in the instituted proceeding. But as we note, that argument relies critically on Patent Owner's proposed construction of "timing control signals," which we reject.

3. Obviousness of Claims 6, 12, 19, and 20 Over Hayashi and Kono

Petitioner challenges claims 6, 12, 19, and 20 as obvious over Hayashi and Kono. Pet. 757, 33–37; Pet. 952, 38–43. Petitioner draws a correspondence between the "optical sensor" recited in the claims and image sensor 607 of Hayashi, the "analog front-end processor" recited in the claims and amplifier 82 of Hayashi, the "analog/digital converter" recited in the claims and A/D converter 83 of Hayashi, and the "timing generator" recited in the claims and driving clock generating circuit 112 of Hayashi. Pet. 757, 34, 36–28; Pet. 952, 39, 41–43. Petitioner acknowledges that "Hayashi does not explicitly state that the timing control signals are supplied to the A/D converter 83," and relies on Kono for the limitations related to using timing control signals to control an analog/digital converter to process analog image signals. Pet. 757, 34; Pet. 952, 39.

Kono discloses a scanner having a separate main board and carriage. Ex. 1008, col. 3, ll. 37–41, col. 5, ll. 6–9. Figure 1 of Kono is reproduced below.

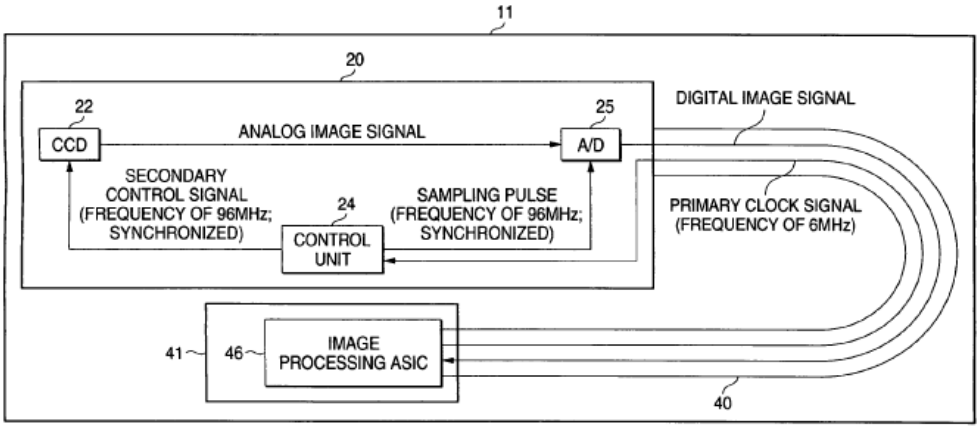

Figure 1 is a schematic diagram that indicates a signal transmission path of a scanner. Control unit 24, which is coupled with both CCD line sensor 22

and A/D converter 25, provides a "shift pulse" signal and a "sampling pulse" signal. Ex. 1008, col. 4, ll. 13–55, col. 5, l. 30 – col. 6, l. 10. The shift pulse signal is transmitted to CCD line sensor 22 to control the timing of generation and extraction of the analog image signal. *Id.* The sampling pulse is transmitted to A/D converter 25 to control the timing of conversion of analog image data to digital image data. *Id.* Petitioner reasons that it would have been obvious to one of ordinary skill in the art to operate Hayashi's scanner system to send signals from the driving clock generating circuit to both the image sensor and A/D converter, as described in Kono, and supports its reasoning with declaration testimony by L. Richard Carley, Ph.D. Pet. 757, 35–36 (citing Ex. 1002 ¶¶ 104–112); Pet. 952, 40–41 (citing Ex. 1102 ¶¶ 91–99).

We conclude that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 6, 12, 19, and 20 as obvious over Hayashi and Kono.

Accordingly, we institute *inter partes* review in IPR2014-00757 of claims 6, 12, 19, and 20 as obvious over Hayashi and Kono under 35 U.S.C. § 103(a). Because the same claims are challenged on the same ground in IPR2014-00952, we decline also to institute a second *inter partes* review of the claims on that ground. *See* 35 U.S.C. § 325(d); 37 C.F.R. § 42.108(b).

4. Obviousness of Claims 2–4, 8, and 14–16 Over Hayashi and Other Art

Petitioner challenges claims 2–4, 8, and 14–16, which relate to the production of scan control signals from scanning instructions, as obvious

over Hayashi and Shiraishi. Pet. 757, 26–33. Petitioner challenges claims 9 and 10, which relate to a memory control logic unit and memory unit, and which depend from claim 8, as obvious over Hayashi, Shiraishi, and Ochiai. Pet. 757, 38–41.

Shiraishi relates to an image reading device that includes an input/output interface through which scanning instructions are received from a host terminal. Ex. 1007 ¶¶ 18–28. Petitioner identifies disclosures in Shiraishi as illustrating the features recited in claims 2–4, 8, and 14–16. Pet. 757, 29–33. Petitioner further contends that one of skill in the art would have combined the teachings of Shiraishi with the image-processing device of Hayashi because Shiraishi discloses further detail of functions that are suggested by Hayashi. *Id.* at 28–29. In challenging claims 9 and 10, Petitioner cites Ochiai's disclosure of coupling a main control logic unit with a memory control logic unit. *Id.* at 39–41. Petitioner supports its analysis with the testimony of Dr. Carley. *See* Ex. 1002 ¶¶ 80, 143–147, 159–161. We have reviewed Petitioner's analysis and are persuaded that Petitioner has made an adequate showing.

We conclude that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 2–4, 8, and 14–16 as obvious over Hayashi and Shiraishi and of prevailing on its challenge to claims 9 and 10 as obvious over Hayashi, Shiraishi, and Ochiai.

Accordingly, we institute *inter partes* review in IPR2014-00757 of claims 2–4, 8, and 14–16 as obvious over Hayashi and Shiraishi under 35 U.S.C. § 103(a). We also institute *inter partes* review in IPR2014-00757 of

claims 9 and 10 on the ground that they would have been obvious over Hayashi, Shiraishi, and Ochiai under 35 U.S.C. § 103(a).

5. Obviousness of Claims 2–4, 8–10, and 14–16 Over Hayashi and Kitani

Petitioner also challenges claims 2–4, 8–10, and 14–16 as obvious over Hayashi and Kitani in its second Petition. Pet. 952, 25–38. We decline to institute *inter partes* review on these grounds, for they rely on teachings from Kitani that Petitioner already identifies as disclosed by Shiraishi and/or Ochiai. *See* 35 U.S.C. §314(a); 37 C.F.R. § 42.108(b). Exercise of our discretion in declining to institute on these grounds is consistent with the authority granted under 35 U.S.C. § 315(d) to manage *inter partes* proceeding and with the objective of "secur[ing] the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1(b).

B. Asserted Grounds Based on Tsuboi and Wada

1. Tsuboi

Tsuboi describes an image-reading device that uses a CCD to collect image data. Ex. 1005 ¶ 1. Figure 4 of Tsuboi is reproduced below.

[FIG. 4]

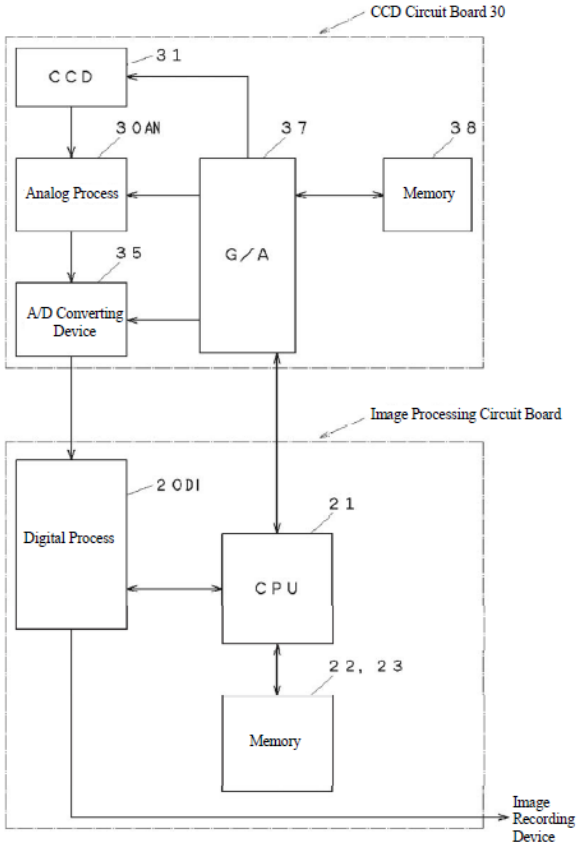

Figure 4 provides a schematic illustration of the image-reading device with components distributed between an image processing circuit board and a CCD circuit board. *Id.* ¶ 36. Petitioner draws a correspondence between (1) the image processing circuit board of Tsuboi and the optical sensor circuit module recited in the claims of the '406 patent, and (2) the CCD circuit board of Tsuboi and the main circuit module recited in the claims. Pet. 757, 42. The image processing circuit board and the optical sensor circuit module are connected by a flexible cable. Ex. 1005 ¶ 25. Similar to the configuration shown in Figure 2 of the '285 patent, Tsuboi discloses that the CCD circuit board includes CCD image sensor 31, analog processing

circuit 30AN, analog-digital converter 35, and "signal processing circuit 37 for controlling the timing with which the CCD 31 is driven and for generating a clock." *Id.* ¶ 36; *see id.* ¶ 3. Signals used to generate that timing information are received from the image processing circuit board. *Id.* ¶ 39. Specifically, in response to a scanning instruction supplied by a user, CPU 21 on main circuit module 20 generates a primary scanning synchronization signal that is transmitted via the flexible cable to signal processing circuit 37, which generates signals that control the timing with which CCD 31 generates and extracts analog image signals. *Id.* ¶ 39, 25.

Petitioner acknowledges that "Tsuboi does not explain in detail how [signal processing] circuit 37 generates the timing control signals in response to the scan control signals," but contends that "one of ordinary skill in the art would have appreciated that the scan control signals would have been processed to generate the timing control signals." Pet. 757, 43. Petitioner supports its contention with declaration testimony by Dr. Carley that it was known at that time to generate timing control signals at an optical sensor circuit module in response to a synchronization signal like the primary synchronization signal in Tsuboi. *Id.* (citing Ex. 1002 ¶¶ 64–67).

2. Wada

Wada describes an image-reading device that uses an image sensor to read a document. Ex. 1006 ¶ 1. Figure 5 of Wada is reproduced below.

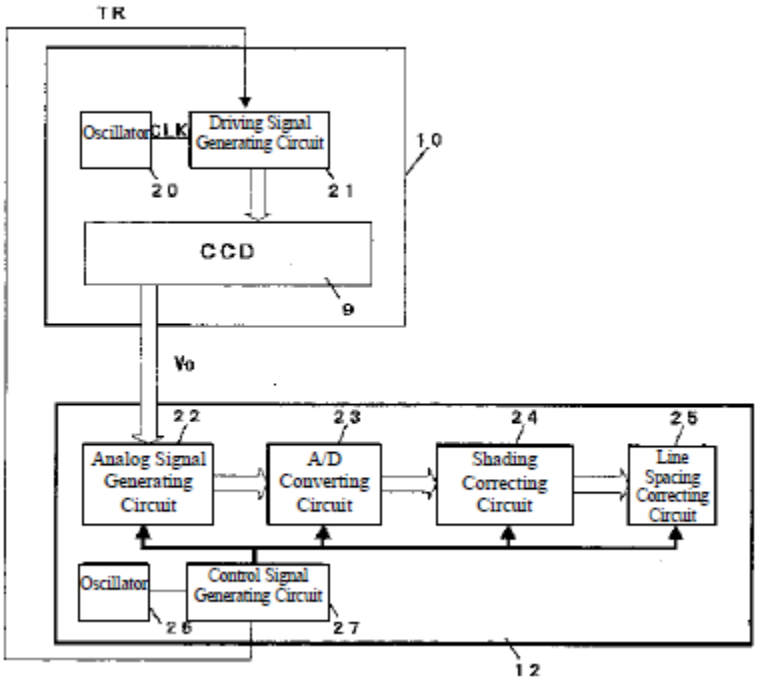

Figure 5 is a block diagram illustrating a structure for the image-reading device, including sensor substrate 10 and processing substrate 12. *Id.* ¶ 15. The sensor substrate includes image sensor (CCD) 9, oscillator 20, and driving signal generating circuit 21. *Id.* The processing substrate includes analog signal generating circuit 22, A/D converting circuit 23, shading correcting circuit 24, line spacing correcting circuit 26, oscillator 26, and control signal generating circuit 27. *Id.* ¶ 17. In response to transmission of a synchronization signal TR from the signal processing substrate to the sensor substrate, the driving signal generating circuit generates signals shift pulse SH, transmission clocks ϕ1 and ϕ2, reset signal ϕRS, and clamp signal ϕCLP for outputting an image signal to the image sensor. *Id.* ¶ 15. Petitioner identifies such signals as "timing control signals." Pet. 757, 44.

3. Obviousness of Claims 1–7, 11–14, and 16–20 Over Tsuboi and Wada

Petitioner contends that the primary scanning synchronization signal disclosed by Tsuboi and the TR synchronization signal disclosed by Wada are "scan control signals." *Id.* at 43, 46–47. Petitioner relies on Wada for disclosing details of how such a synchronization signal may be used to generate timing control signals, such as pulse SH and transmission clocks ϕ1 and ϕ2. *Id.* at 43–45. Petitioner reasons that Tsuboi teaches that the "received scan control signals do not comprise any timing control signals" because the signals for controlling CCD 31 are generated by signal processing circuit 37 on an optical circuit sensor module. *Id.* at 46. Petitioner similarly reasons that Wada teaches the same limitation because the timing control signals are generated by a driving signal generating circuit on an optical sensor circuit module in response to receipt of synchronization signal TR. *Id.* at 46–47.

These contentions are similar to the contentions advanced by Petitioner for its Hayashi-based grounds, namely that a scan control signal cannot also be a "timing control signal" if timing control signals are generated in response to information it carries. For reasons similar to those expressed *supra* in our analysis of the Hayashi-based grounds, we are persuaded that Petitioner has made a sufficient showing to support its contention that the combination of Tsuboi and Wada discloses "scan control signals [that] do not comprise any timing control signals," as recited in independent claims 1, 7, and 13.

We have reviewed Petitioner's claim charts and supporting citations for claims 1–7, 11–14, and 16–20 (Pet. 757, 45–54), and conclude that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge of those claims as obvious over Tsuboi and Wada.

Accordingly, we institute an *inter partes* review in IPR2014-00757 of claims 1–7, 11–14, and 16–20 on the ground that they would have been obvious over Tsuboi and Wada under 35 U.S.C. § 103(a).

4. Obviousness of Claims 8–10 and 15 Over Tsuboi, Wada, and Other Art

Petitioner challenges claims 8 and 15 as obvious over Tsuboi, Wada, and Shiraishi. Pet. 757, 55–57. Petitioner also challenges claims 9 and 10 as obvious over Tsuboi, Wada, Shiraishi, and Ochiai. *Id.* at 57–59. Petitioner presents reasoning similar to that considered above for combining Shiraishi and/or Ochiai with Hayashi to meet the limitations of claims 8–10 and 15. Namely, Petitioner relies on Shiraishi's disclosure of a scanning instruction associated with an image resolution, a brightness level, or a scanning range as recited in claims 8 and 15, and relies on Ochiai's disclosure of a separate memory control logic unit with an image pre-processor as recited in claims 9 and 10.

We conclude that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge of claims 8 and 15 as obvious over Tsuboi, Wada, and Shiraishi; and of prevailing on its challenge of claims 9 and 10 as obvious over Tsuboi, Wada, Shiraishi, and Ochiai.

Accordingly, we institute an *inter partes* review in IPR2014-00757 of claims 8 and 15 on the ground that they would have been obvious over Tsuboi, Wada, and Shiraishi under 35 U.S.C. § 103(a). We also institute an *inter partes* review in IPR2014-00757 of claims 9 and 10 on the ground that they would have been obvious over Tsuboi, Wada, Shiraishi, and Ochiai under 35 U.S.C. § 103(a).

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that *inter partes* review is *instituted* in IPR2014-00757 with respect to the following grounds:

(1) claims 1, 5, 7, 11, 13, 17, and 18 as anticipated by Hayashi under 35 U.S.C. § 102(b);

(2) claims 6, 12, 19, and 20 as obvious over Hayashi and Kono under 35 U.S.C. § 103(a);

(3) claims 2–4, 8, and 14–16 as obvious over Hayashi and Shiraishi under 35 U.S.C. § 103(a);

(4) claims 9 and 10 as obvious over Hayashi, Shiraishi, and Ochiai under 35 U.S.C. § 103(a);

(5) claims 1–7, 11–14, and 16–20 as obvious over Tsuboi and Wada under 35 U.S.C. § 103(a);

(6) claims 8 and 15 as obvious over Tsuboi, Wada, and Shiraishi under 35 U.S.C. § 103(a); and

(7) claims 9 and 10 as obvious over Tsuboi, Wada, Shiraishi, and Ochiai under 35 U.S.C. § 103(a);

FURTHER ORDERED that *inter partes* review is *not instituted* for any claims in IPR2014-00952;

FURTHER ORDERED that no other ground than those specifically instituted above is authorized for the *inter partes* review; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '285 patent is hereby instituted in IPR2014-00757 commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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