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Paper 25
Entered: September 19, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BLACKBERRY CORPORATION,
Petitioner,

v.

NXP B.V.,
Patent Owner.

Case IPR2013-00232
Patent 5,639,697

Before JENNIFER S. BISK, TRENTON A. WARD, and BRIAN P. MURPHY, *Administrative Patent Judges.*

MURPHY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

On April 2, 2013, Blackberry Corporation ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–4 of U.S. Patent No. 5,639,697 ("the '697 patent"). Paper 1 ("Pet."). On July 3, 2013, NXP B.V. ("Patent Owner") filed the Patent Owner's Preliminary Response to the Petition. Paper 7 ("Prelim. Resp."). On September 30, 2013, we issued the Decision on Institution of *Inter Partes* Review of claims 1–4 pursuant to 35 U.S.C. § 314, determining that the information presented in the Petition and cited exhibits demonstrated a reasonable likelihood Petitioner would prevail with respect to claims 1–4 of the '697 patent. Paper 9 ("Dec.").

On December 16, 2013, Patent Owner filed the Patent Owner's Response (Paper 14, "PO Resp."). On March 3, 2014, Petitioner filed its Reply to Patent Owner's Response. Paper 15 ("Pet. Reply"). Neither party filed a motion to exclude evidence. Both parties requested oral hearing, and the oral hearing was held on June 2, 2014. Paper 23 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is entered pursuant to 35 U.S.C. § 318(a). We conclude that Petitioner has shown by a preponderance of the evidence that claims 1–4 are unpatentable under 35 U.S.C. §§ 102(a) and 103.

A. Related Proceedings

The '697 patent is the subject of a federal district court case between the parties, titled *NXP B.V. v. Research In Motion Ltd.*, Case No. 6:12-cv-498 (M.D. Fla.). In addition to this petition, on October 1, 2013, we instituted *inter partes* review based on Petitioner's challenges to the patentability of certain claims of Patent Owner's U.S. Patent No. 6,501,420 B2 (IPR2013-00233). Our Final Decision in that proceeding is being

entered concurrently with this Decision.

B. The '697 Patent

The '697 patent is titled "Dummy Underlayers For Improvement In Removal Rate Consistency During Chemical Mechanical Polishing." Ex. 1001. The '697 patent relates generally to methods of fabricating integrated circuits ("IC") on a semiconductor wafer, and it discloses that maintaining a consistent height across the wafer surface is crucial to the fabrication process. *Id.* at 1:16–36. Chemical Mechanical Polishing ("CMP") is a known method for achieving a planar wafer surface. *Id.* at 1:27–30. CMP involves applying a polishing slurry of oxidizing chemicals and microscopic abrasive particles to a wafer surface, in combination with a rotating polishing pad and pressure, to "polish" —i.e., controllably remove material from — the wafer surface. *Id.* at 1:37–52.

The '697 patent discloses that the amount of material removed during CMP depends, in part, on the pattern density of raised areas on the surface of the wafer layer being polished. *Id.* at 1:53–57. The '697 patent invokes Preston's law, which states that the removal rate of material during CMP is directly proportional to the down force exerted on the wafer and inversely proportional to the surface area of the wafer in contact with the polisher. *Id.* at 1:61–2:9, 5:12–15. The problem noted is that the removal rate during CMP can be inconsistent because the concentration of raised areas can vary across the surface of a wafer layer (*id.* at 2:30–50, Figs. 1A & 1B), as well as from layer to layer and IC product to IC product (*id.* at 2:4–9). The '697 patent, therefore, describes and claims a method for improving removal rate consistency during CMP by determining the pattern density of raised areas on a wafer surface as a ratio of raised surface area to total surface area of the

wafer. *Id*. at 3:26–38, 5:26–6:13, 7:19–42.

Figure 3C of the ’697 patent is reproduced below:

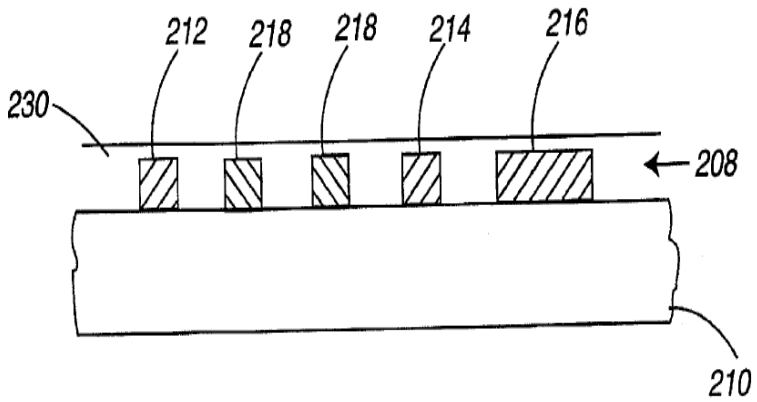

FIG. 3C

Figure 3C depicts CMP process resulting in planar insulating surface layer.

Figure 3C, reproduced above, shows a plurality of dummy raised lines 218 placed between active conductive traces 212 and 214 on wafer surface layer 208. Ex. 1001, 6:30–33. Active conductive traces are raised areas or lines electrically coupled to associated elements of the ICs being fabricated on semiconductor substrate 210. *Id.* at 6:40–43. Dummy raised lines 218 are added to increase the density of raised areas on the wafer surface, but they are not electrically coupled to associated circuit elements. *Id.* at 6:33–36, 44–47. The number and surface area of dummy raised lines added to a wafer surface “depend[] upon the percentage of pattern density of topography desired.” *Id.* at 6:33–36. For example, dummy raised lines may be added between active conductive traces such that the dummy lines and active traces, combined, constitute between 40%–80% of the entire surface area of a wafer. *Id.* at 3:57–61, 6:10–13. After the active conductive traces and dummy raised lines have been formed on the wafer surface in

accordance with the determined pattern density, oxide layer 230 is deposited over them. *Id.* at 6:52–57. The oxide layer on the wafer surface is planarized using CMP. *Id.* at 6:57–60.

Claim 1 of the '697 patent is illustrative and reproduced below.

> 1. A method of fabricating a semiconductor wafer having at least one integrated circuit, the method comprising the steps of:
>
> forming a multiplicity of active conductive traces on a surface of a substrate of the wafer, the active conductive traces each being arranged to electrically couple associated elements of an associated integrated circuit on the wafer, there being gaps between adjacent ones of the active conductive traces;
>
> *determining a standard uniform pattern density for the surface of the semiconductor wafer*;
>
> forming a multiplicity of dummy raised lines on the surface of the substrate in the gaps, wherein the dummy raised lines are not arranged to electrically couple any elements in the integrated circuit, the multiplicity of dummy raised lines and the multiplicity of active conductive traces *forming the standardized uniform pattern density over the surface of the substrate*;
>
> depositing an insulating layer over the active conductive traces to electrically insulate the active conductive traces; and,
>
> polishing the surface of the insulating layer to provide a planar surface on the wafer, whereby the dummy raised lines cooperate with the active conductive traces to improve standardized polishing of the wafer.

Ex. 1001, 7:59–8:16 (emphasis added).

C. Prior Art Relied Upon in the Petition

Petitioner relies upon the following prior art references:

Nowak	US 4,916,514	April 10, 1990	Ex. 1008
Rostoker	US 5,265,378	Nov. 30, 1993	Ex. 1006
Lee	US 5,441,915	Aug. 15, 1995	Ex. 1005
Chesebro	US 5,636,133	June 3, 1997	Ex. 1004
Juengling	US 5,981,384	Nov. 9, 1999	Ex. 1007
Ueno	JP. Pat. Pub. No. H07-74175	Mar. 17, 1995	Ex. 1002
Ueno	Certified English Translation of Ex. 1002	Mar. 17, 1995	Ex. 1003

Pet. 3.

D. Grounds of Unpatentability

We instituted *inter partes* review based on the following grounds of unpatentability:

Reference[s]	**Basis**	**Claims Challenged**
Ueno	§ 102(a)	1-4
Chesebro and Rostoker	§ 103	1 and 2
Chesebro, Rostoker, and Nowak	§ 103	3 and 4
Lee and Rostoker	§ 103	1–4
Lee, Rostoker, and Juengling	§ 103	2

Dec. 23.

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, we construe claim terms according to their broadest reasonable interpretation in light of the patent specification. 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Under the broadest reasonable interpretation standard, we assign claim terms their ordinary and customary meaning, as understood by one of ordinary skill in the art, in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation omitted). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). We construe the disputed claim term below in accordance with these principles.

The parties offer competing interpretations of the following claim limitation: "determining a standard uniform pattern density for the surface of the semiconductor wafer," as set forth in claim 1. Pet. 6–7; PO Resp. 13–17. Petitioner advocates that the claim limitation means a flexible standard for reducing variation in pattern density across the surface of a single wafer layer, from layer to layer, or from IC product to IC product. Pet. 6. Patent Owner advocates that the claim limitation means a standard for achieving a consistent depth of material removal during a particular CMP action for all

"commonized" wafer layers. PO Resp. 14–16. We address the parties' arguments in context of the '697 patent claim language and written description.

1. "pattern density for the surface of the semiconductor wafer"

"[A] claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citation omitted). The '697 patent uses lexicography to define the portion of the claim limitation that recites a "pattern density for the surface of the semiconductor wafer" as: "The pattern density of topography is defined as the ratio of the overall surface area of raised areas on a wafer surface to the total surface area of the wafer." Ex. 1001, 4:60–63. This definition is consistent with the repeated references in the '697 patent to wafer surface topography as having raised areas, the combined surface area of which is a ratio or percentage of the total surface area of the wafer. *Id.* at Abstract, 3:34–38, 57–61, 4:54–63, 6:26–40. Therefore, we adopt the definition recited above for the portion of the claim limitation reciting a "pattern density for the surface of the semiconductor wafer." *See* PO Resp. 16.

2. *"determining a standard[ized] uniform pattern density"*

a."standardized"[1]

[1] Amended application claim 1, as allowed by the Examiner, recited "determining a *standardized* uniform pattern density." PO Resp. 13–14; Ex. 2007, 89, 105 (emphasis added). Claim 1 of the '697 patent, as issued, however, recites "determining a *standard* uniform pattern density." Ex. 1001, 8:1 (emphasis added). Although a certificate of correction due to the United States Patent and Trademark Office's error has not been made of record, we construe the claim language as written at the time of allowance,

Claim 1 of the '697 patent recites a method of fabricating "at least one integrated circuit" on "*a* semiconductor wafer" by forming active traces, dummy raised lines, and an insulating layer "on *a* surface of *a* substrate of the wafer." Ex. 1001, 7:59–8:16 (emphases added). In a patent claim, "a" means "one or more." *See 01 Communique Lab., Inc. v. LogMeIn, Inc.*, 687 F.3d 1292, 1297 (Fed. Cir. 2012) ("As a general rule, the words 'a' or 'an' in a patent claim carry the meaning of 'one or more.'") (citation omitted). Therefore, we frame the analysis of the word "standardized" in the claim language at issue in the context of fabricating at least one IC device on one or more surface layers of one or more semiconductor wafers. Pet. Reply 2–4. Express recognition of this claim construction principle helps resolve the disparate views of the parties over the meaning of "standardized."

In the claim phrase at issue, "standardized" modifies "pattern density." Claim 1 further recites that "a multiplicity of dummy raised lines" and "active conductive traces" form "*the* standardized uniform pattern density over the surface of the substrate." Ex. 1001, 8:6–9 (emphasis added). The phrase determining a "standardized" uniform pattern density, therefore, instructs one skilled in the art to determine the surface area ratio of active conductive traces and dummy raised lines on one or more surface layers of one or more wafers according to some standard.

The plain and ordinary meaning of "standard" is "a level of quality, achievement, etc., that is considered acceptable or desirable." Ex. 3001

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i.e., standardized. *See Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1354 (Fed. Cir. 2003) (A claim can be construed to resolve obvious errors only if (1) the correct construction "is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims.").

(Merriam-Webster Dictionary Online, http://www.merriam-webster.com/dictionary/standard (last visited September 4, 2014)). The '697 patent does not describe how to determine a "standardized" pattern density (Tr. 20), but it does describe "commonizing" pattern density to reduce variation in pattern density across the surface of a single wafer layer, from layer to layer within a wafer, or from IC product to IC product on different wafers, to improve CMP removal rate consistency. *E.g.*, Ex. 1001, 3:13–18 ("[D]ummy raised areas . . . *commonize* the pattern density of topography from layer to layer of an integrated circuit, as well as from product to product.") (emphasis added), 3:23–29 ("The overall surface area of the raised areas . . . typically varies from layer to layer. In order to *commonize* the pattern density of topography from layer to layer of an integrated circuit and from product to product, dummy raised areas are added to the same layers on which active conductive traces are situated.") (emphasis added), 7:39–42 ("It should be clear that dummy raised lines may be added to a single layer of a wafer in order to achieve a desired pattern density of topography on that layer alone."). In the context of the entire '697 patent disclosure, "commonizing" pattern density refers to reducing variation in pattern density (*see* Ex. 1010 (Decl. of Ron Maltiel) ¶ 17), or, similarly, increasing the commonality of pattern density (*see* Ex. 2006 (Decl. of Dr. Bruce Smith) ¶ 15 (citing Ex. 1001, 1:17–21)), on one or more surface layers of one or more semiconductor wafers to be polished.

The claimed method step permits flexibility in how to reduce pattern density variation in order to accommodate different concentrations of raised surface areas (Ex. 1001, 2:4–9, 3:23–25, 5:26–29), different fabrication processing requirements (*id.* at 2:51–61, 5:1–5, 6:61–7:18), and various

device requirements and operating conditions. A person skilled in the art would understand, in particular, that the claim phrase in question "does not refer to a single specific pattern density value that is used for all workpieces undergoing CMP." Ex. 2006 ¶ 85. For example, the '697 patent discloses a standard that is flexible enough to determine different pattern densities for different surface layers of a wafer. Ex. 1001, 5:34–39; PO Resp. 17; Pet. Reply 3–4; Ex. 1021, 7; Ex. 1022, 6–7 (¶¶ 56–57); Tr. 29. It is also flexible enough to determine a pattern density for a single surface layer of a wafer (Ex. 1001, 7:39–42; Pet. Reply 2–4; Ex. 1021, 7; Ex. 1022, 5 (¶ 55)), which reduces pattern density variation across the wafer surface in comparison to the wafer surface without any dummy raised areas in the gaps between active conductive traces. *See* Ex. 1001, 7:39–42, Figs. 3A–C, 4a–e; PO Resp. 4; Ex. 2006 ¶¶ 38, 39, 98, 101, 115; Tr. 6, 8. We conclude that the claimed method step incorporates a flexible standard for reducing variation in pattern density when determining the surface area ratio of active conductive traces and dummy raised areas for one or more surface layers on one or more wafers to be polished.

Patent Owner's proposed construction, which requires "consistent material removal when the wafer undergoes a particular CMP action" (PO Resp. 16), is misplaced.[2] Patent Owner's expert, Dr. Bruce Smith, explains

[2] When claim 1 was amended during prosecution, Patent Owner's counsel remarked in similar fashion:

> Accordingly, by maintaining a fixed material removal rate, it is easier to control the depth at which material is removed from the surface of the substrate. In addition, maintaining substantially the same standardized pattern density on all layers of a plurality of distinct types of integrated circuits enables the CMP process used to planarize

that "'[p]articular' means the CMP operation is performed with a predetermined set of process parameters such as polishing pressure, polishing time, polishing slurry and polishing pad." Ex. 2006 ¶ 85 (footnote omitted). Particular CMP process parameters, however, are not recited in the method of claim 1.[3]

Claims 7 and 8 of the '697 patent, by way of comparison with claim 1, are limited to fabricating a wafer having a plurality of active layers (claim 7 f)) or fabricating a plurality of distinct types of ICs formed on distinct multi-layer wafers (claim 8), where the pattern density determined for each surface layer and IC is "substantially the same." Ex. 1001, 10:1–14; *see also id.*at 5:60–62. In the fabrication methods of claims 7 and 8, determining that the pattern density will be "substantially the same" for each surface layer and IC reduces variation to an effective minimum, i.e., there will be a single pattern density for all surface layers on all wafers to be polished. When CMP process parameters are "particular" or "fixed" for such fabrication methods, a consistent material removal rate is achieved in accordance with Preston's

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all integrated circuits to remain fixed, thereby efficiently improving the CMP fabrication process.

Ex. 2007, 92. This comment focuses on a preferred embodiment and the goal of improving CMP removal rate consistency using fixed CMP process parameters, rather than on the step of determining a standard for the arrangement of active and dummy raised lines on one or more wafer surfaces of one or more wafers.

[3] The polishing step of claim 1 takes place after the determining step: "whereby the dummy raised lines cooperate with the active conductive traces to improve standardized polishing of the wafer." Ex. 1001, 8:13–16. This method step refers to an improvement in removal rate consistency during CMP polishing of a wafer surface (*id.* at 2:51–61, 7:23–26), but it does not impose particular CMP process parameters as limitations on the determining step.

law. *Id.* at 5:62–67. Given the absence of determining "substantially the same" pattern density as a limitation in claim 1, and given the further absence of a limitation reciting particular CMP process parameters, we decline to limit the step of "determining a standardized uniform pattern density" to require consistent material removal when the wafer undergoes a particular CMP action. *See In re Van Geuns*, 988 F.2d at 1184.

b. "uniform"

The '697 patent states that the dummy raised areas may be formed as blocks, lines, or dots of different shapes and sizes to fill the gaps between active conductive traces. Ex. 1001, 3:43–47, 6:18–20. The '697 patent further states that the dummy raised areas may be arranged on the surface of an integrated circuit in a pattern that may be uniform or non-uniform. *Id.* at 3:39–43, 6:20–25. A non-uniform pattern is described as dummy lines or shapes "scattered about the surface of the integrated circuits . . . in a non-uniform pattern." *Id.* at 6:20–22. Independent claims 5 and 7, by way of comparison, claim "determining a standardized pattern density," which would include both uniform and non-uniform patterns. We determine, therefore, that the word "uniform" modifies "pattern" in claim 1, and limits the pattern of raised areas on a wafer surface to a "uniform pattern" in accordance with the plain and ordinary meaning of uniform.[4]

3. Conclusion

For the reasons given above, we conclude that the broadest reasonable interpretation of the phrase "determining a standard uniform pattern density

[4] Merriam Webster's dictionary online defines "uniform" as "having always the same form, manner, or degree: not varying or variable." Ex. 3002 (Merriam-Webster Online Dictionary, http://www.merriam-webster.com/dictionary/uniform (last visited September 4, 2014)).

for the surface of the semiconductor wafer" (claim 1) is "determining a uniform arrangement of active conductive traces and dummy raised areas on a surface of a semiconductor wafer as a ratio of the overall surface area of raised areas on the wafer surface to the total surface area of the wafer, so as to reduce variation in pattern density with respect to one or more surface layers of one or more wafers to be polished."

B. Anticipation of Claims 1–4 by Ueno

Petitioner contends that Ueno anticipates claims 1–4 of the '697 patent. Pet. 16–20. Petitioner supports its argument with the declaration of its expert, Mr. Ron Maltiel, and citations to Ueno that correspond to all limitations in claims 1–4. *Id.* (citing Ex. 1003; Ex. 1010 ¶¶ 44–47); *see* Reply Declaration of Ron Maltiel, Ex. 1024 ¶¶ 17–20. Patent Owner opposes, relying on the declaration of its expert, Dr. Smith. PO Resp. 18–24 (citing Ex. 2006 ¶¶ 92–97, 100). Patent Owner argues the limitations "determining a standard uniform pattern density for the surface of the semiconductor wafer" and "forming the standardized uniform pattern density" are not disclosed in Ueno. *Id.* Patent Owner does not contest Ueno's disclosure of the other limitations of claim 1 or separately argue dependent claims 2–4. *Id.* Based on our review of the record evidence, we are persuaded by Petitioner's arguments that Ueno anticipates claims 1–4 of the '697 patent. We, therefore, concentrate our discussion on the disputed claim limitation construed above.

1. Ueno

Ueno describes a method of manufacturing multilayer planarized semiconductor devices. Ex. 1003, Abstract, ¶ 1. Ueno teaches that any gaps between active conductive wiring, which exceed a chosen dimension, e.g. about 2 microns, should be filled with raised non-conductive dummy structures before CMP planarization. Ex. 1010 ¶ 44 (citing Ex. 1003, Abstract, ¶¶ 1, 6, 8–9, 12, Figs. 1a, 2). Ueno provides examples where the width of the active conductive wiring and dummy structures is about 1 micron each, and therefore the 2-micron gaps filled by the dummy structures are reduced to about 0.5 to 1 micron. Ex. 1003 ¶¶ 9, 12; Ex. 1024 ¶¶ 20–21. Ueno's Figures 1a and 2 illustrate Ueno's arrangement of active and dummy wiring and are reproduced below. Figure 1a depicts a cross-sectional view of active and dummy wiring.

Ueno's Figure 2 is reproduced below.

[Fig. 2]

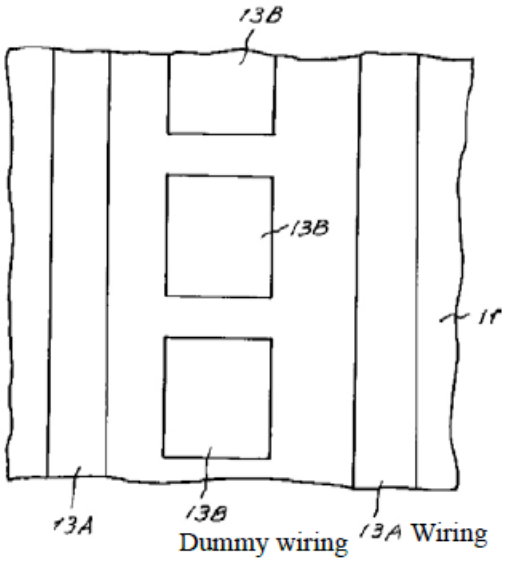
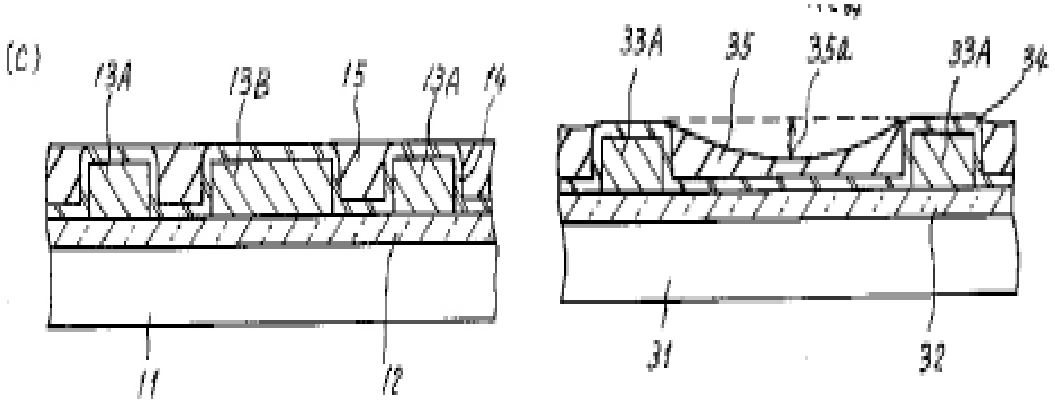


Figure 2 depicts top view of active and dummy wiring.

Figures 1a and 2, above, illustrate the location, shape, and spacing of dummy wiring 13B and active wiring 13A, which are formed at the same time by applying common photolithography and etching processes. Ex. 1003 ¶ 8. A plasma nitride film layer 14 covers the active and dummy wiring, and an interlayer insulation film 15 is deposited over the plasma nitride layer. *Id*. at Abstract, ¶ 10, Fig. 1b; *see also id.* ¶¶ 12, 17, Figs. 3b, 4b. Ueno describes, in particular, how adding dummy raised areas in the gaps between active conductive wiring causes the pattern density of raised surface area to be "increased." *Id.* ¶ 10; *see also id.* Figs. 3a–c, ¶ 12 ("[D]ummy wiring 23B is arranged in large intervals between wiring 23A to *increase the density* of plasma nitride film 24 on its upper surface.") (emphasis added). By increasing the surface area density of active and dummy wiring, which is covered by plasma nitride on its upper surface, Ueno improves CMP polishing of the wafer to provide "full flattening" of the wafer surface. *Id*. at Abstract, ¶¶ 2, 6, 10, 12, 17, Figs. 1c, 3c, 4c. The result is shown in Figure 1c reproduced (below left) in comparison to Figure 5 without dummy structures (below right).



Ueno Figure 1c (left) and Figure 5 (right) showing a CMP planarized surface layer with and without dummy structures, respectively.

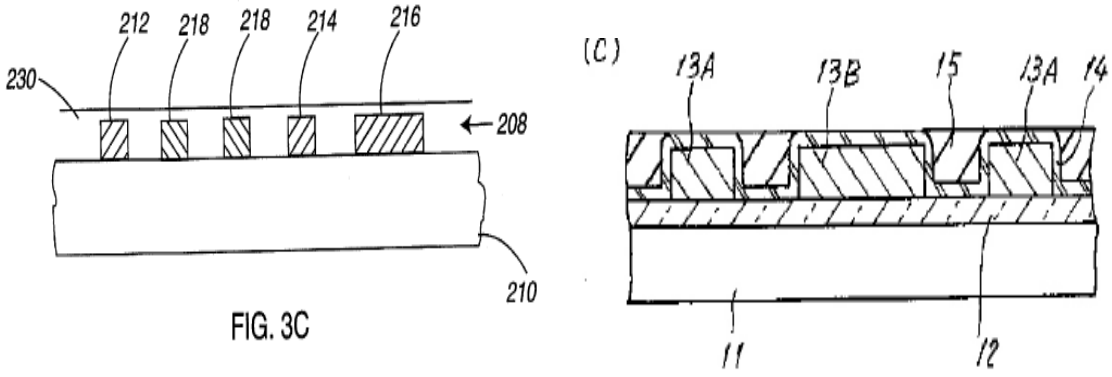
Figure 1c, reproduced above left, illustrates a CMP planarized surface layer resulting from Ueno's method of adding dummy wiring 13B in between active wiring 13A. Ueno's method increases pattern density on the wafer surface as compared to Figure 5, above right, which illustrates a CMP planarized surface layer without dummy structures between active wiring 33A. *Compare* Ex. 1003, Fig. 1c, *with id.* at Fig. 5; *see also id.* ¶¶ 5, 6, 9, 12; Ex. 1010 ¶ 45. Figure 5 illustrates the problem of having large gaps that result in pits or "dishing" of the wafer surface layer during CMP. *See* Ex. 1010 ¶ 44.

2. Anticipation Analysis

We begin our analysis by repeating our claim construction, namely, that the claims 1–4 require "determining a uniform arrangement of active conductive traces and dummy raised areas on a surface of a semiconductor wafer as a ratio of the overall surface area of raised areas on the wafer surface to the total surface area of the wafer, so as to reduce variation in pattern density with respect to one or more surface layers of one or more wafers to be polished."[5] Ueno discloses a single wafer surface layer, similar to the embodiment disclosed in Figures 3A–C of the '697 patent.

A comparison of the '697 patent's Figure 3C, below left, to Ueno's Figure 1(c), below right, illustrates the similarity.

Claims 2 and 3 depend from claim 1. Claim 4 depends from claim 3.



Planarized wafer surface shown in ’697 patent Figure 3C (left) and Ueno Figure 1(c) (right), each containing dummy raised structures

Figure 3C of the ’697 patent (above left), in terms of our claim construction, shows an “arrangement of active conductive traces [212, 214, and 216] and dummy raised areas [218] on a surface of a semiconductor wafer.” Ueno Figure 1(c) (above right) also shows an “arrangement of active conductive traces [13A] and dummy raised areas [13B] on a surface of a semiconductor wafer.” Both figures show a “uniform” arrangement of raised areas on the semiconductor surface. Figure 2 of Ueno shows a uniform pattern of rectangular dummy raised areas regularly spaced apart to fill gaps between active wiring lines. Ex. 1003, Fig. 2; *see also* Ex. 1024 ¶ 21.

Ueno’s method also teaches one of skill in the art “to reduce variation in pattern density with respect to one or more surface layers on one or more wafers to be polished,” in much the same way as taught by the ’697 patent. As explained above, Ueno adds dummy raised areas between active conductive lines according to a set of gap width, spacing, and line width dimensions to increase the pattern density of the raised surface area, thereby reducing variation of pattern density and the potential for “dishing” across the surface of the wafer. Ex.1003 ¶¶ 6, 8–10, 12, 17, Figs. 1c, 3c, 4c, 5;

Pet. 17; Ex. 1010 ¶¶ 44–45; Pet. Reply 6–7; Ex. 1024 ¶¶ 17, 20–21. Ueno's method and rationale for increasing pattern density on a wafer surface is comparable to the '697 patent's "commonized" pattern density that reduces variation across a wafer surface. Ex. 1001, 7:39–42, Figs. 3A–C, 4a–e; Pet. 17; Ex. 1010 ¶¶ 44–45; PO Resp. 4; Ex. 2006 ¶¶ 38, 39, 98, 101, 115; Pet. Reply 2.

Patent Owner argues that Ueno does not disclose determining a "standardized" pattern density because Ueno uses a plasma nitride "stopper" layer to control CMP planarization, rather than a method where the same depth of material is removed from every layer of every product during CMP, using a fixed set of CMP process parameters. PO Resp. 18–24 (citing Ex. 2006 ¶¶ 92–97). Patent Owner's argument rests squarely on its proposed claim construction, which we have declined to adopt. The claim phrase at issue does not require a fixed set of CMP process parameters to remove the same depth of material from every wafer surface layer to be polished, as argued by Patent Owner. PO Resp. 19 (citing Ex. 2006 ¶¶ 94, 96).[6]

Patent Owner further argues that Ueno takes into account "only" the spacing (gap width) between active lines, but not the width of active and dummy wiring, and therefore teaches a "constant pattern density" for all layers and wafers but not a "standardized" pattern density. PO Resp. 21–22 (citing Ex. 2006 ¶¶ 94–95, 97, 100). Patent Owner's argument is not

[6] Patent Owner takes the argument a step further, stating that Ueno's use of a plasma nitride stopper layer would lead one of ordinary skill in the art away from the claimed invention of the '697 patent. PO Resp. 23; Ex. 2006 ¶ 95. Ueno's use of a plasma nitride stopper layer *and* raised dummy areas in the gaps between active wiring are not mutually exclusive or inconsistent. Ex. 1003, ¶¶ 10–13; Pet. Reply 7–8; Ex. 1024 ¶¶ 25–26.

consistent with the '697 patent claims and written description. Patent Owner's argument presumes a "constant" pattern density, where all layers of one or more multi-layer wafers are determined to have the same pattern density. Such a constant pattern density may be recited in claims 7 and 8 of the '697 patent,[7] but it is not recited in claim 1. *See* Ex. 1001, 7:39–42, 7:59–8:18, 10:1–14. Moreover, as discussed above and explained by Petitioner's expert, Mr. Maltiel, Ueno discloses to one of ordinary skill in the art how to reduce variation in pattern density (or increase commonality of pattern density) by setting design rules for gap width spacing, active line width, and dummy structure width. Pet. Reply 5–7; Ex. 1024 ¶¶ 20–24. Ueno's method, therefore, teaches one of ordinary skill in the art to determine the overall surface area of raised active lines and dummy areas on a wafer surface "as the ratio of the overall surface area of raised areas on a wafer surface to the total surface area of the wafer" (Ex. 1001, 4:61–63) — the desired pattern *density* expressly described by Ueno. Ex. 1003 ¶¶ 10, 12. Ueno's method, like the method claimed in the '697 patent, improves CMP polishing consistency and achieves the "full flattening" shown in Ueno's several illustrated examples. Ex. 1003 ¶¶ 9–12, Figs. 1(a)–(c), 3 (a)–(c), 4 (a)–(c).

In sum, Ueno's method arranges raised dummy structures in a uniform pattern to fill gaps between active conductive lines according to specified gap width, spacing, and line width dimensions to determine a pattern density ratio of raised surface area on the wafer surface to be polished. Ueno's method reduces variation in pattern density across the

[7] Claims 7 and 8 recite that each active layer of a wafer or each discrete type of integrated circuit, respectively, has "substantially the same" pattern density. Ex. 1001, 10:1–14.

wafer surface and improves consistency of CMP planarization of the wafer surface. Therefore, we are persuaded by Petitioner's evidence and arguments as to the anticipation of all limitations in claims 1-4 by Ueno. Pet. 16–20 (citing Ex. 1003; Ex. 1010 ¶¶ 44–47); Ex. 1024 ¶¶ 17–20. We are not persuaded by Patent Owner's evidence and arguments. PO Resp. 18–24 (citing Ex. 2006 ¶¶ 92–97, 100).

Based on our review of both Petitioner's and Patent Owner's arguments and supporting evidence, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1–4 of the '697 patent are anticipated by Ueno.

C. Obviousness of Claims 1 and 2 over Chesebro and Rostoker

Petitioner asserts that claims 1 and 2 of the '697 patent are obvious over Chesebro in view of Rostoker under 35 U.S.C. § 103. Pet. 20–27. Petitioner supports its argument with Mr. Maltiel's Declaration and citations to Chesebro and Rostoker that correspond to all limitations in claims 1 and 2. *Id.* (citing Ex. 1004; Ex. 1010 ¶¶ 49–50, 52–54, 56–66); s*ee* Ex. 1024 ¶¶ 27–28). Patent Owner opposes, relying on Dr. Smith's Declaration, and argues the limitations of "determining a standard uniform pattern density for the surface of the semiconductor wafer" and "forming the standardized uniform pattern density" are not taught by the combination of Chesebro and Rostoker. PO Resp. 24–30 (citing Ex. 2006 ¶¶ 102, 104–106). Patent Owner does not contest Petitioner's evidence that the proposed combination teaches the other limitations of claim 1. *Id.* Petitioner does not separately argue dependent claim 2. Pet. 20–27. Based on our review of the record evidence, we are persuaded by Petitioner's arguments that claims 1 and 2 of the '697 patent are obvious over Chesebro or Chesebro and Rostoker. We

again concentrate our discussion on the disputed claim limitation construed in section A. above.

1. Chesebro

Chesebro describes the modification of a semiconductor IC pattern by adding "fill shapes" to each layer of a semiconductor wafer to correct for fabrication process deviations and to make the "local pattern density more uniform." Ex. 1004, Abstract, 1:33–38, 2:21–48; Ex. 1010 ¶ 49. Chesebro's fill shapes have no electrical function, but they "reduce variations in local pattern density." Ex. 1004, 2:2–5. Chesebro teaches that reducing variation in pattern density is important because fabrication processes such as CMP may be affected by non–uniform variations in local pattern density. *Id.* at 1:50–2:5, 2:21–34; Ex. 1010 ¶ 49.

Chesebro starts with an "original" IC design and, using a computer-implemented-design technique, creates "areas-not-to-fill" that represent the active conductive areas on each layer of an IC that will not be filled with dummy fill shapes. Ex. 1004, 2:35–38, 4:3–5, Figs. 3, 5; Ex. 1010 ¶ 50; Ex. 1024 ¶ 27. The computed areas-not-to-fill is then "complemented" to generate "areas-to-fill" with dummy fill shapes, in between the active conductive areas. Ex. 1004, 2:40–46, 4:5–9, 4:20–24, 4:65–67; Ex. 1010 ¶ 51; Ex. 1024 ¶ 27. Figure 5 illustrates Chesebro's technique.

Chesebro's Figure 5 is reproduced below.

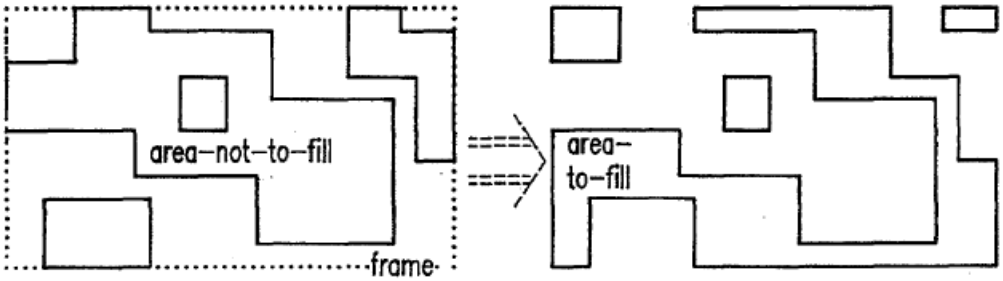


FIG.5

Figure 5 illustrates complemented dummy areas-to-fill.

Chesebro selects the dummy fill pattern to have "the same pattern density as the densest parts of the as-designed shapes on the polysilicon level" of the original IC design. Ex. 1004, 5:27–30, 5:36–40; Ex. 1010 ¶¶ 52–53; Ex. 1024 ¶ 27. The dummy fill pattern is composed of "a regular array of unit cells," as shown in Figure 7 below. Ex. 1004, 5:36–40.

Chesebro's Figure 7 is reproduced below.

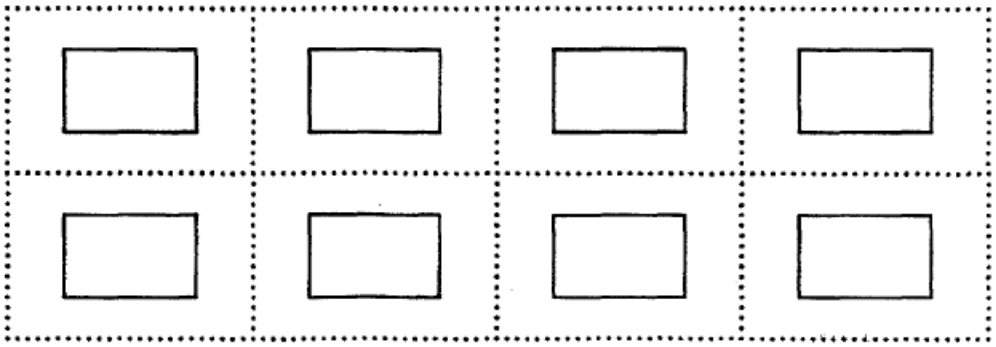


FIG.7

Figure 7 illustrates regular array of dummy fill unit cells.

Chesebro describes an example where the pattern density of active lines on a wafer layer in the original IC is 25%. *Id.* Chesebro chooses a dummy fill pattern density of 25%, which is composed of unit cells each

consisting of 2 μm x 2 μm squares in 4 μm x 4 μm frame[8] as shown in Figure 7 above. *Id.*; Ex. 1010 ¶ 53; Ex. 1024 ¶ 27. The dummy fill pattern of unit cells achieves the desired 25% local pattern density across the wafer surface layer. Ex. 1004, 5:27–40; Ex. 1010 ¶ 53. The process of creating areas-not-to-fill complemented by areas-to-fill with a dummy fill pattern is repeated for each layer of the semiconductor wafer so that the resulting design may be used to fabricate the IC. Ex. 1004, 2:35–48, 4:9–12; Ex. 1010 ¶ 54; Ex. 1024 ¶ 27.

2. Obviousness Analysis

Obviousness under 35 U.S.C. § 103 requires an assessment of (1) the "level of ordinary skill in the pertinent art," (2) the "scope and content of the prior art," (3) the "differences between the prior art and the claims at issue," and (4) any evidence of "secondary considerations" of nonobviousness such as "commercial success, long-felt but unsolved needs, failure of others, etc." *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007) (quoting *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)). A party who petitions the Board for a determination of obviousness must show that "'a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)). We assess Petitioner's evidence and argument according to this standard.

[8] Raised area/total surface area = (2 μm x 2 μm)/(4 μm x 4 μm) = 4/16 = 25%. Ex. 1010 ¶ 53.

Mr. Maltiel opines that at the time of the '697 patent filing date in January 1996, one of ordinary skill in the art would have been familiar with computer implemented design programs, such as disclosed in Chesebro, to design IC devices. Ex. 1010 ¶¶ 54, 58, 59. Patent Owner does not contest Petitioner's argument and evidence that one of ordinary skill in the art of IC fabrication at the time[9] would have understood from Chesebro, or from Chesebro and Rostoker, that Chesebro's IC design method would have included active conductive traces in the areas-not-to-fill and dummy raised areas made of the same material in the areas-to-fill. Pet. 21–23 (citing Ex. 1010 ¶¶ 50, 54, 57–59); PO Resp. 24–29 (citing Ex. 2006 ¶¶ 102, 104–106). Thus, there is no dispute that Chesebro or Chesebro and Rostoker discloses an "arrangement of active conductive traces and dummy raised areas on a surface of a semiconductor wafer," in accordance with our claim construction.

There also is no dispute that Chesebro discloses a "uniform" arrangement of raised areas on a semiconductor surface, including the "regular array" of unit cells shown in Figure 7 used to fill the "areas-to-fill" shown in Figure 10. Ex. 1004, 5:27–40, 6:13–24; Pet 23–24; Ex. 1010 ¶ 53; PO Resp. 26. The dispute between the parties again concerns the interpretation of determining a "standardized" pattern density. *See* PO Resp. 26–29.

[9] Mr. Maltiel provides an in-depth discussion of the knowledge and skill level of a person of ordinary skill in the art at the time the '697 patent application was filed in January 1996. Ex. 1010 ¶¶ 18-40. He also describes his own education and experience in the semiconductor industry between 1977 and 1996. *Id.* at ¶¶ 4-14.

Petitioner and its expert, Mr. Maltiel, contend that Chesebro's method reduces variation in pattern density on a single layer of a wafer as well as among multiple layers. Pet. 23–24 (citing Ex. 1010 ¶¶ 60–61). Patent Owner contends that by "**individually selecting** the uniform pattern densities for plural layers or wafers, with no relationship between the uniform pattern density of different layers (or wafers)," Chesebro "cannot be suggestive of the claimed *standardized* uniform pattern density that applies to multiple layers on a wafer or layers of multiple wafers." PO Resp. 26–27; Ex. 2006 ¶¶ 101–102. The thrust of Patent Owner's argument is based on its proposed claim construction, which *excludes* determining a standardized pattern density for a single layer of a wafer. We have declined to adopt Patent Owner's proposed construction. Patent Owner's argument also is inconsistent with the written description of the '697 patent and Patent Owner's acknowledgement that the claim limitation in question encompasses the ability to determine different pattern densities for different layers of a multi-layer wafer or wafers. Ex. 1001, 5:34–44; PO Resp. 17; Ex. 2006 ¶ 102; Pet. Reply 3–4; Tr. 29.

We agree with Petitioner's expert, Mr. Maltiel, that by combining an original IC design with a dummy fill pattern at each layer, particularly a fill pattern having the same pattern density as that of the densest part of the original IC design, Chesebro teaches a reduction in the variation in that layer's pattern density. *See* Ex. 1010 ¶ 61. We also credit Mr. Maltiel's opinion that a person of skill in the art would have recognized that Chesebro's process steps "describe a simultaneous filling of this multi-level structure, which would be most easily and beneficially executed by using the same fill pattern for every level in the entire structure" as a matter of prudent

cost and process efficiency. *See* Ex. 1024 ¶ 28. Thus, we are persuaded that Chesebro teaches a process for using the same fill pattern on each layer of a multi-layer wafer, thereby reducing pattern density variation between multiple layers. *See* Ex. 1010 ¶ 61.

Chesebro teaches one of skill in the art to determine pattern density "as a ratio of the overall surface area of raised areas on the wafer surface to the total surface area of the wafer," by describing a percentage, e.g., 25%, for the raised areas-not-to-fill and the raised areas-to-fill on each wafer surface layer of the IC to be fabricated. Ex. 1004, 1:52–56, 5:27–40. The raised areas of the selected pattern density in Chesebro are determined so as to reduce variation across the wafer surface, with the effect of improving CMP polishing. *Id.* at 1:62–2:6, 2:29–33; Ex. 1010 ¶ 65.

To the extent one of ordinary skill in the art might have required more detail regarding the CMP process, Rostoker describes CMP in detail. *E.g.*, Ex. 1006, 1:43–50, 1:56–59, 5:32–52, Fig. 1. We also credit Mr. Maltiel's opinion that a person of ordinary skill in the art "would have been motivated to use Chesebro's addition of dummy structures to reduce variation and improve wafer planarization of deposited layers using the CMP process described in Rostoker." Ex. 1010 ¶ 66 (referring to ¶¶ 36–39). With regard to Patent Owner's argument that Rostoker's use of a "stop" structure would have led one of skill in the art away from the process claimed in the '697 patent (PO Resp. 28–29), we determine, as we did above with the challenge based on Ueno, that the use of a stop structure and raised dummy areas in the gaps between active wiring are not mutually exclusive or inconsistent. *See* Ex. 1024 ¶¶ 25–26 (citing Ex. 1006, 5:58–6:42; Ex. 1003 ¶ 4). Therefore, we are persuaded by Petitioner's evidence and

arguments as to the obviousness of claims 1-4 by Chesebro and Rostoker. Pet. 20–27 (citing Ex. 1004; Ex. 1010 ¶¶ 49–50, 52–54, 56–66); Ex. 1024 ¶¶ 27-28. We are not persuaded by Patent Owner's evidence and arguments. PO Resp. 24–30 (citing Ex. 2006 ¶¶ 102, 104–106).

For the reasons stated above and based on our review of both Petitioner's and Patent Owner's arguments and supporting evidence, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1 and 2 of the '697 patent are obvious over Chesebro or Chesebro and Rostoker.

D. Obviousness of Claims 3 and 4 over Chesebro, Rostoker, and Nowak

1. Nowak

Nowak describes the use of "dummy conductors" to achieve planarized semiconductor layers. Ex. 1008, Abstract, 2:5–26, 47–62; Ex. 1010 ¶ 68. Nowak teaches one of skill in the art to choose a maximum allowable spacing between raised metallization lines and then to add dummy conductors in those spaces where the maximum is exceeded. Ex. 1008, 3:3–7, 8–14, 60–67, 4:39–44, 5:18–22, 29–32, Figs. 2 & 3; Ex. 1010 ¶ 68. Nowak further describes an additive planarization technique where the insulating layer covering the active and dummy conductors is formed so as to minimize surface peaks and valleys that result from gaps between metallization, thereby improving surface planarity. Ex. 1008, Abstract, 2:16–21, 3:1–14, 20–29, 3:60–4:2, 39–49, 5:18–22, 29–32, Figs. 2, 3, 5A & 5B; Ex. 1010 ¶ 68.

Nowak specifies that for ease of fabrication and to avoid extra time and cost, the dummy and active conductors should be made of the same

material, either conductive metal or polysilicon, and should have the same thickness. Ex. 1008, Abstract, 2:22–26, 62–68, 4:28–29, 5:34–41; Ex. 1010 ¶ 69. For the same reason, Nowak states that active and dummy conductors should be patterned with the same mask and formed from the same fabrication steps. *See* Ex. 1008, Abstract, 2:22–26, 62–68, 4:28–29, 5:34–41; Ex. 1010 ¶ 69. Nowak teaches that once the pattern is formed on the substrate, it should be covered with an insulation layer, such as silicon dioxide, so as to minimize surface peaks and valleys. Ex. 1008, 3:15–33, 67–4:2, 45–49, 6:1–5; Ex. 1010 ¶ 70.

2. Analysis

Claim 3 depends from claim 1 and recites that the dummy raised lines are formed "from the same material" and "applied at the same time" as the active conductive traces, and that the insulating layer covers the "dummy raised lines in addition to the active conductive traces." Ex. 1001, 8:21–26. Claim 4 depends from claim 3 and further limits the active conductive traces and dummy raised lines to a "metallic material" and the insulating layer to "an oxide material." *Id.* at 27–31. Petitioner argues that claims 3 and 4 are obvious over the combination of Chesebro, Rostoker, and Nowak. Pet. 27–31 (citing Ex. 1004; Ex. 1006; Ex. 1008; Ex. 1010 ¶¶ 50, 54, 57-59, 62-64, 69, 71-76). Patent Owner opposes and argues claims 3 and 4 together. PO Resp. 30–34 (citing Ex. 1008; Ex. 1010 ¶ 68; Ex. 2006 ¶¶ 109-111, 114-115).

Petitioner emphasizes that Nowak expressly teaches an IC fabrication method where the "dummy conductors are formed with the same mask and by the same steps as the active conductors and, accordingly, are of the same material and have the same thickness as the active conductors." Pet. 28

(citing Ex. 1008, Abstract, 2:21–26, 62–68). This description from Nowak is close to an *in haec verba* description of the "same material" and "applied at the same time" limitations of claim 3. Petitioner further states that Figure 3 of Nowak teaches an insulating layer that "overlies the signal conductors 20*a* and 20*b* and the dummy conductors 22." Pet. 28 (citing Ex. 1008, 3:22–25, 67–4:2, 6:1–5); Ex. 1010 ¶¶ 73–74. Nowak's Figure 3 illustrates the IC device structure in cross-sectional view. Ex. 1008, Fig. 3.

Mr. Maltiel opines that:

> [A] person of ordinary skill, after reading Nowak, would have understood that IC fabrication is made easier and more efficient by fabricating an IC with dummy structures using the same material with the same thickness for both active conductive traces and dummy raised structures, and from forming both at the same time, in the same way. Accordingly, this person of ordinary skill would have recognized that these same efficiency benefits accrue to the fabrication process of Chesebro and, therefore, would have been motivated to incorporate Nowak's method of using the same material for both active conductive traces and dummy raised lines and applying both on the surface at the same time.

Ex. 1010 ¶ 72. Mr. Maltiel's opinion is consistent with Chesebro's IC design strategy, which recognizes the need to provide "an efficient method" for modifying an IC design (Ex. 1004, 2:21–22) that will be fabricated using photolithography to pattern the IC devices and CMP to planarize wafer surfaces (*id.* at 1:62–65). *See* Ex. 1024 ¶¶ 31–32. Mr. Maltiel's opinion is further supported by Ueno, which describes forming active and dummy wiring "at the same time," and is further evidence of well-understood processing steps for forming active and dummy structures at the same time from the same material using the same photolithography mask sets. Ex. 1003 ¶ 8. Therefore, we credit Mr. Maltiel's opinion as providing a

sound rationale for why one of ordinary skill in the art would have used processing steps described in Nowak for the fabrication of active lines and dummy structures in an IC designed according to Chesebro.

Patent Owner argues that Nowak does not remedy the asserted deficiency of Chesebro with respect to "determining a standardized uniform pattern density." *See* PO Resp. 30–34. We decline to adopt Patent Owner's construction of the disputed claim limitation (section A), and conclude that Chesebro discloses the process step of "determining a standardized uniform pattern density" (section C). We are not persuaded, therefore, by Patent Owner's argument.

Patent Owner further argues, in reliance on Dr. Smith's Declaration, that one of ordinary skill would not have combined Nowak with Chesebro and Rostoker because Nowak teaches an additive planarization technique, not CMP, to planarize a wafer surface. PO Resp. 30–34 (citing Ex. 2006 ¶¶ 109–111). Patent Owner argues that Nowak teaches away from including Rostoker in the asserted prior art combination, because Nowak's additive planarization technique renders CMP unnecessary. PO Resp. 33 (citing Ex. 1010 ¶ 68; Ex. 2006 ¶¶ 110–111). Patent Owner concludes, therefore, that the asserted combination does not render claim 3 obvious over Chesebro, Rostoker, and Nowak.

We are persuaded by Petitioner that Patent Owner's argument fails to account for developments in semiconductor fabrication processing techniques, including CMP, that occurred after Nowak's May 1988 patent application filing date but prior to the January 1996 filing date of the '697 patent. *See* Pet. Reply 10–11. As Mr. Maltiel explains, the type of dummy structures used in Nowak served the same planarization purpose as dummy

structures used in Ueno, Chesebro, and other later-filed prior art references, but with increased benefit. Ex. 1024 ¶ 31. "[B]y starting with a more even, equally-dense, surface which helped to avoid dishing during etchback and CMP procedures," one of ordinary skill would have known that Nowak's "well-known" technique for forming active lines and dummy structures at the same time from the same material "could reasonably [be] combined with the more modern planarization techniques of Chesebro, Rostoker and/or Lee." *Id.* at ¶¶ 31–32 (citation omitted). Dr. Smith's contrary testimony on this point does not persuade us otherwise. *See* Ex. 2006 ¶¶ 110–112.

We conclude that one of ordinary skill in the art in January 1996, rather than being led away from using Nowak's efficient fabrication technique for forming active lines and dummy structures at the same time using the same material followed by an oxide layer, reasonably would have used Nowak's technique to further benefit from the later-developed CMP planarization technique referenced in Chesebro and described in Rostoker.[10]

For the reasons stated above and based on our review of both Petitioner's and Patent Owner's arguments and supporting evidence, we conclude that Petitioner has shown by a preponderance of the evidence that claims 3 and 4 of the '697 patent are obvious over Chesebro, Rostoker, and Nowak.

E. Obviousness of Claims 1–4 by Lee and Rostoker

Petitioner argues that the combination of Lee and Rostoker would have rendered claims 1–4 obvious to one of ordinary skill in the art as of the January 1996 filing date of the '697 patent. Pet. 32–37 (citing Ex. 1005; Ex.

[10] Patent Owner does not contest Petitioner's evidence that Nowak discloses the claimed insulating layer covering "the dummy raised lines in addition to the active conductive traces." *See* PO Resp. 30–34.

1010 ¶¶ 80-90). Patent Owner opposes. PO Resp. 34–39 (citing Ex. 1005; Ex. 2006 ¶¶ 58, 104, 113-115, 117, 119). Our analysis follows.

1. Lee

Lee is directed to fabricating a planarized multilevel interconnection system for IC devices. Ex. 1005, 1:11–15. In Lee, large gaps between conductive metal lines on each level are filled with dummy lines, where the gap is equal to or greater than three times the feature size or the width of the conductive lines. *Id.* at 2:38–56. Insulating layers, applied using a spin-on glass technique that includes formation of silicon oxide, are provided between metal layers. *Id.* at 2:56–57, 4:50–61, Fig. 7B. The top surface of an oxide layer is planarized using a chemical process called reactive ion etching, or "etch back." *Id.* at 1:51–56, 4:62–66. In Figure 7C, Lee shows oxide layers 46 and 48 after chemical etch back (removal of surface material) with trifluoromethane (CHF_3) or carbon tetrafluoride (CF_4).

Lee's Figure 7C is reproduced below.

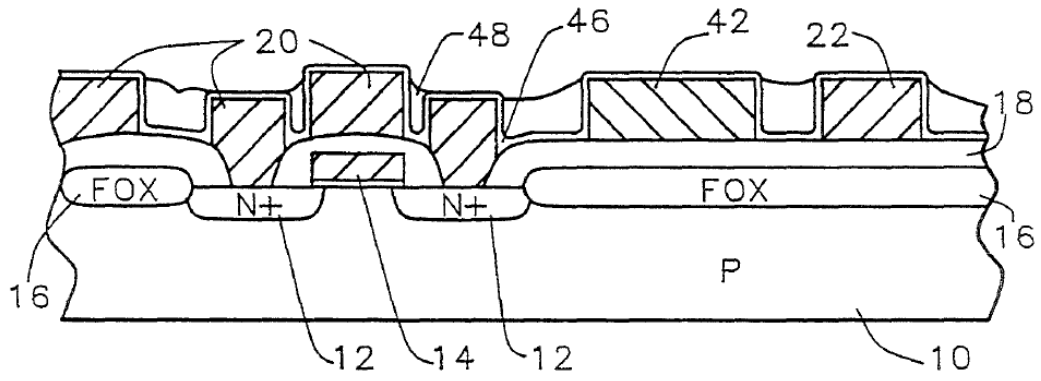


Figure 7C depicts oxide layers 46 and 48 after etch back.

Figure 7C, above, shows metal lines 20 and 22 covered with a relatively thin oxide layer 46 and the areas in between covered with a

relatively thicker oxide layer 46, 48. Lee does not reference or teach CMP as an acceptable method of planarization.

2. Analysis

Claim 1 of the '697 patent recites "polishing the surface of the insulating layer to provide a planar surface on the wafer, whereby the dummy raised lines cooperate with the active conductive traces to improve standardized polishing of the wafer." Ex. 1001, 8:13-16. Petitioner's expert, Mr. Maltiel, opines that one of ordinary skill would have known that "in certain instances" CMP would have been preferable to etch back as a planarization technique and could have been "predictably substituted" for Lee's etch back process. Ex. 1010 ¶ 88; Pet. 35–36. Mr. Maltiel opines that one of ordinary skill would have been motivated to do so by Rostoker, without further explanation. Ex. 1010 ¶ 88. Mr. Maltiel does not describe precisely why CMP would have been preferable to etch back as used in Lee's fabrication system, or what particular disclosure in Rostoker would have prompted one of ordinary skill to make the asserted substitution with a reasonable expectation of success. *Id.* ¶¶ 88–89.

Patent Owner's expert, Dr. Smith, responds that one of ordinary skill would not have had a reason to substitute CMP for Lee's etch back technique because "CMP does not offer the selectivity of removal between materials necessary for Lee." Ex. 2006 ¶ 117; *see also id.* at ¶¶ 113–116. As shown in Figure 7C of Lee, a relatively thin oxide layer (46) is deposited on metal lines (20) to isolate them electrically. Ex. 1005, Fig. 7C. A spin-on glass layer (48) overcoats the oxide layer and metal lines to fill in gaps between the lines. *Id.* at ¶ 117. Dr. Smith explains that chemical etch back removes spin-on glass (48) at a higher rate than oxide (46), "as seen by the

entire layer 46 remaining[,] [a] CMP process would not discriminate between these two oxide layers (46 and 48) and would cause removal of film 46 and quite possibly the metal (20)." *Id.* (citation omitted). Dr. Smith further emphasizes the importance of etch back selectivity between metal lines (20) and oxide layers (48 and 52), as shown in Figures 9C and 10B, which is necessary to avoid unwanted removal of the metal. *Id.*

Mr. Maltiel does not contradict or refute Dr. Smith's critique of the asserted substitution of Rostoker's CMP technique for Lee's chemical etch back, asserting only that one of skill in the art would replace spin-on glass with a simple oxide layer. Ex. 1024 ¶ 34 (citations omitted). Mr. Maltiel, however, does not explain why one of skill in the art would want to replace spin-on glass with an oxide layer in Lee's fabrication system. He also does not account for the selectivity of Lee's etch back technique to remove spin-on-glass layer 48 at a higher rate than oxide layer 46 while avoiding unwanted removal of metal. Therefore, we are not persuaded by Petitioner's argument and evidence that one of ordinary skill would have had a reason to substitute Rostoker's CMP technique for Lee's etch back technique with a reasonable expectation of success.

For the reasons stated above and based on our review of both Petitioner's (Pet. 32–37) and Patent Owner's (PO Resp. 34–39) arguments and supporting evidence, we conclude that Petitioner has not shown by a preponderance of the evidence that claims 1–4 of the '697 patent are obvious over Lee and Rostoker.

F. Obviousness of Claim 2 over Lee, Rostoker, and Juengling

Claim 2 of the '697 patent depends from claim 1 and recites "the dummy raised lines are formed at least partially from elements selected from

the group consisting of a multiplicity of dots, a multiplicity of blocks, and a multiplicity of line segments." Ex. 1001, 8:17-20. Petitioner's arguments and evidence asserting the obviousness of claim 2 (Pet. 37-39) do not address further the deficiency of the asserted combination of Lee and Rostoker as explained in section E above. In particular, Petitioner argues that Juengling teaches the use of varying-size blocks or segmented dummy features. Pet. 38-39. Petitioner does not argue that Juengling teaches one of ordinary skill to use CMP of an oxide layer in place of Lee's spin-on glass etch back technique. *Id.* Therefore, for the same reasons discussed in section E, we conclude Petitioner has not shown by a preponderance of the evidence that claim 2 of the '697 patent is obvious over Lee, Rostoker, and Juengling.

III. CONCLUSION

For the reasons given above, we are persuaded that Petitioner has shown by a preponderance of evidence that claims 1–4 of the '697 patent are unpatentable under 35 U.S.C. §§ 102(a) and 103.

IV. ORDER

It is

ORDERED that claims 1–4 of U.S. Patent No. 5,639,697 have been shown to be *unpatentable* by a preponderance of the evidence;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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